SUPER®

SUPER X5DL8-GG
SUPER X5DLR-8G2+
SUPER X5DLR-8G2

USER'S MANUAL

Revision 1.0c

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Printed in the United States of America

Preface

About This Manual

This manual is written for system integrators, PC technicians and knowledgeable PC users. It provides information for the installation and use of the SUPER X5DL8-GG/X5DLR-8G2+/X5DLR-8G2 serverboard. At launch, the SUPER X5DL8-GG/X5DLR-8G2+/X5DLR-8G2 supported single or dual Intel® Xeon™ 1.50 - 3.20 GHz processors at a 533/400 MHz front side bus. Refer to the motherboard specifications pages on our web site (http://www.supermicro.com/Product_page/product-m.htm) for updates on supported processors. This product is intended to be professionally installed.

Manual Organization

Chapter 1 begins with a checklist of what should be included in your mainboard box, describes the features, specifications and performance of the motherboard and provides detailed information about the chipset.

Chapter 2 begins with instructions on handling static-sensitive devices. Read this chapter when you want to install the processor and DIMM memory modules and when mounting the mainboard in the chassis. Also refer to this chapter to connect the floppy and hard disk drives, SCSI drives, the IDE interfaces, the parallel and serial ports, the front control panel functions, the speaker and the keyboard.

If you encounter any problems, see **Chapter 3**, which describes troubleshooting procedures for the video, the memory and the setup configuration stored in CMOS. For quick reference, a general FAQ (Frequently Asked Questions) section is provided. Instructions are also included for contacting technical support. In addition, you can visit our web site at www.supermicro.com/techsupport.htm for more detailed information.

Chapter 4 includes an introduction to BIOS and provides detailed information on running the CMOS Setup utility.

Appendix A gives information on BIOS error beep codes.

Appendix B provides POST BIOS checkpoint codes.

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Chapter 1: Introduction

Chapter 2: Installation

Chapter 3: Troubleshooting

Chapter 4: AMIBIOS

Appendices:

Chapter 1
Introduction

1-1 Overview

Checklist

Congratulations on purchasing your computer motherboard from an acknowledged leader in the industry. Supermicro boards are designed with the utmost attention to detail to provide you with the highest standards in quality and performance.

Please check that the following items have all been included with your motherboard. If anything listed here is damaged or missing, contact your retailer.

One (1) Supermicro Mainboard

One (1) ribbon cable for IDE devices

One (1) floppy ribbon cable

One (1) COM port cable

One (1) USB cable

One (1) I/O backpanel shield

Two (2) fan/heatsink assemblies (Fan-042 - retail only)

Two (2) sets of heatsink retention clips (SKT-095-604, 4 total)

One (1) Supermicro CD or diskettes containing drivers and utilities

One (1) User's/BIOS Manual

SCSI Accessories

One (1) 68-pin LVD SCSI cable (retail only)

One (1) set of SCSI driver diskettes

One (1) SCSI manual

Contacting Supermicro

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Notes

Figure 1-1. SUPER X5DL8-GG Image

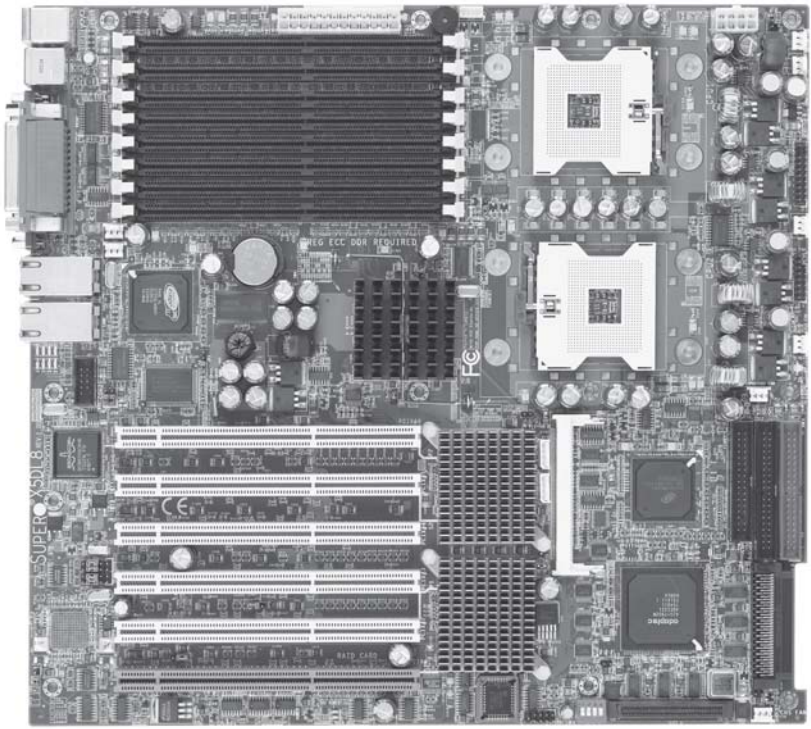
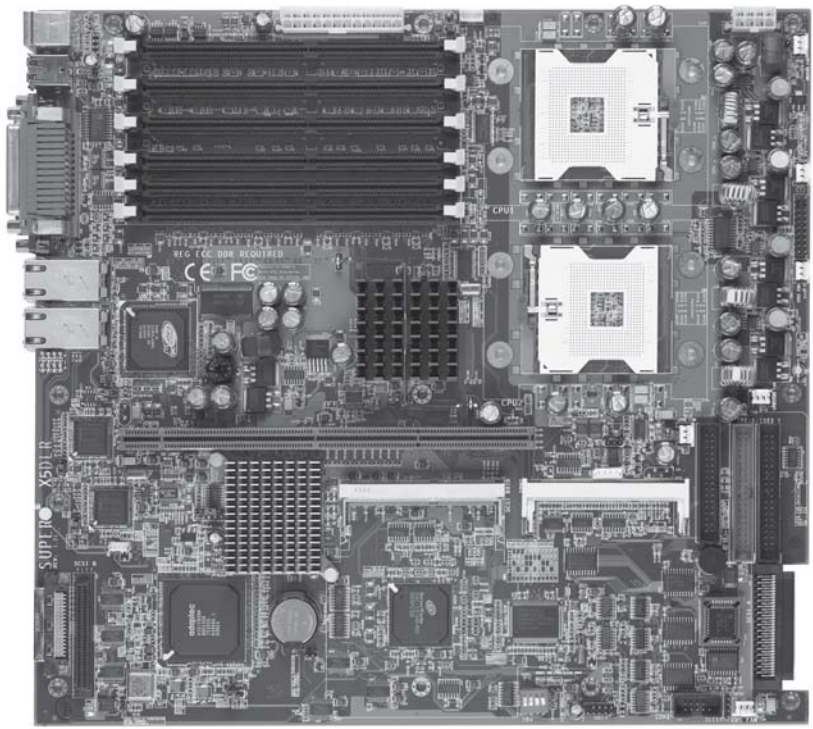
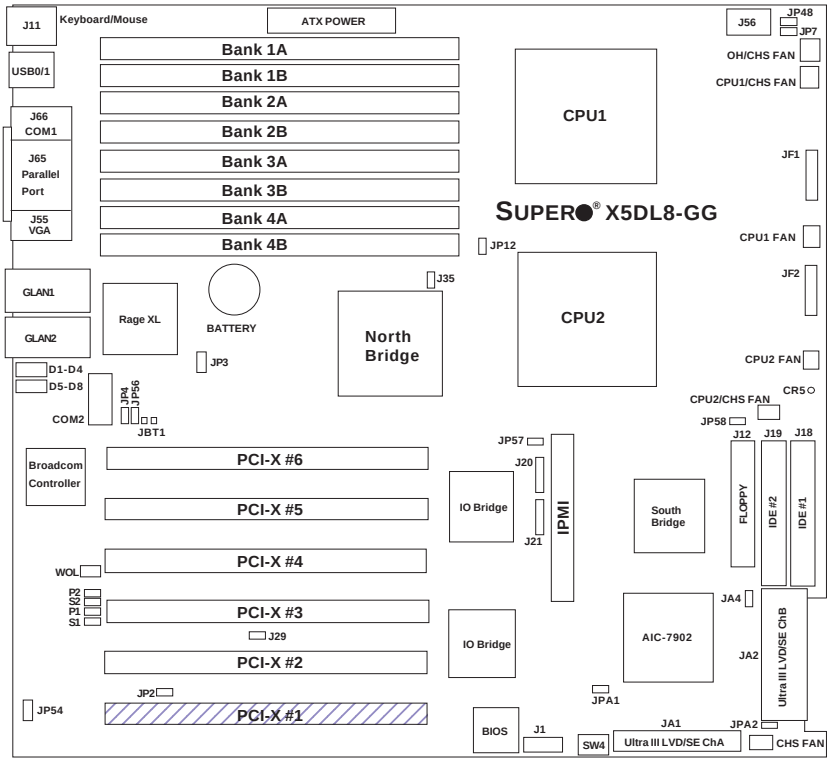


Figure 1-2. SUPER X5DLR-8G2 Image



Note: the X5DLR-8G2+ has the same layout but has 1) no parallel (printer) port and 2) a standard PCI-X slot.

Figure 1-3. SUPER X5DL8-GG Layout
(not drawn to scale)



Note: DIP Switch 4 sets the CPU Core/Bus Ratio (see Section 2-7).
CR5 is a power LED indicator (see Section 2-6).
Jumpers not noted are for test purposes only.
IPMI is optional.

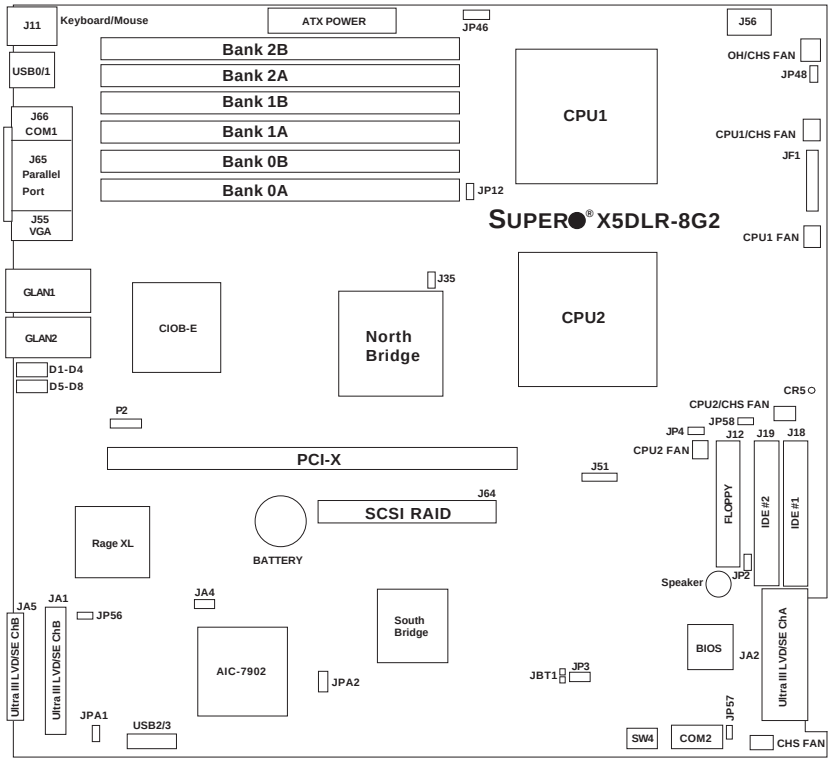
Also see Chapter 2 for the locations of the I/O ports and Front Control Panel (JF1/JF2) connectors and for details on jumper settings and pin definitions.

X5DL8-GG Quick Reference

Jumper	Description	Default Setting
J29	33 MHz PCI Enable/Disable	Open (Disabled)
J35	Spread Spectrum	Open (Disabled)
JA4	SCSI Enable/Disable	Pins 1-2 (Enabled)
JBT1	CMOS Clear	See Chapter 2
JP2	PCI 3.3V Standby En/Dis	Pins 1-2 (Disabled)
JP3	Watch Dog	Pins 2-3 (NMI)
JP4	GLAN2 Enable/Disable	Pins 1-2 (Enabled)
JP7	Main Power Override	Open (Normal)
JP12	System Bus Speed	Pins 1-2 (Auto)
JP48	Chassis/Overheat Fan Select	Open (Overheat)
JP54	GLAN1 Enable/Disable	Pins 1-2 (Enabled)
JP56	VGA Enable/Disable	Pins 1-2 (Enabled)
JP58	Fan Detection Select	Open (CPU Fan)
JPA1/A2	SCSI Channel A/B Termination	Open (Terminated)
P1/2, S1/2	PCI-X Speed Settings	See Section 2-8

Connector	Description
ATX POWER	Primary ATX Power Connector
BANK1A-BANK4B	Memory (RAM) Slots
COM1/COM2	COM1/COM2 Serial Port Connector/Header
CPU1/CPU2	CPU 1 and CPU2 Sockets
CPU/CHS/OH FAN	CPU/Chassis/Overheat Fan Headers
D1-D8	Debug LEDs
GLAN1/GLAN2	Ethernet Ports
J1	USB2/3 Headers
J11	PS/2 Keyboard/Mouse Ports
J12	Floppy Disk Drive Connector
J18, J19	IDE #1/#2 Hard Disk Drive Connectors
J20/J21	IPMB/SMB Headers
J56	Processor Power Connector
J65	Parallel Printer Port
J219	IPMI Slot (for IPMI daughter card)
JA1/JA2	Ultra320 LVD SCSI CH A/B Connector
JF1	Front Control Panel Connector
JF2	Speaker/HD LED Connectors
JP46	Third Power Supply Fail Header
JP57	Chassis Intrusion Header
USB0/1	Universal Serial Bus Ports
VGA	VGA Display (Monitor) Port
WOL	Wake-on-LAN Header

Figure 1-4. SUPER X5DLR-8G2 Layout*
(not drawn to scale)



Note: the X5DLR-8G2+ has the same layout but has 1) no parallel (printer) port and 2) a standard PCI-X slot.

X5DLR-8G2+/X5DLR-8G2 Quick Reference

Jumper	Description	Default Setting
J35	Spread Spectrum	Open (Disabled)
JA4	SCSI Enable/Disable	Pins 1-2 (Enabled)
JBT1	CMOS Clear	See Chapter 2
JP2	Speaker Enable/Disable	Closed (Enabled)
JP3	Watch Dog	Pins 2-3 (NMI)
JP12	System Bus Speed	Pins 1-2 (Auto)
JP48	Chassis/Overheat Fan Select	Open (Overheat)
JP56	VGA Enable/Disable	Pins 1-2 (Enabled)
JP58	Fan Detection Select	Open (CPU Fan)
JPA1/A2	SCSI Channel A/B Termination	Open (Terminated)
P2	PCI-X Speed Settings	See Section 2-8

Connector	Description
ATX POWER	Primary ATX Power Connector
BANK1A-BANK3B	Memory (RAM) Slots
COM1/COM2	COM1/COM2 Serial Port Connector/Header
CPU1/CPU2	CPU 1 and CPU2 Sockets
CPU/CHS/OH FAN	CPU/Chassis/Overheat Fan Headers
D1-D8	Debug LEDs
GLAN1/GLAN2	Ethernet Ports
J1	USB2/3 Headers
J11	PS/2 Keyboard/Mouse Ports
J12	Floppy Disk Drive Connector
J18, J19	IDE #1/#2 Hard Disk Drive Connectors
J51	SMB Header
J56	Processor Power Connector
J64	SCSI RAID Card Slot
J65	Parallel Printer Port
JA1/JA2	Ultra320 LVD SCSI CH A/B Connector
JF1	Front Control Panel Connector
JP46	Third Power Supply Fail Header
JP57	Chassis Intrusion Header
USB0/1	Universal Serial Bus Ports
USB2/3	Universal Serial Bus Headers
VGA	VGA Display (Monitor) Port

Motherboard Features

CPU

- Single or dual Intel® Xeon™ 1.50 - 3.20 GHz 604/603-pin processors with a 1 MB cache at a front side (system) bus speed of 533/400 MHz.

Note: Please refer to the motherboard specifications pages on our web site for updates on supported processors (http://www.supermicro.com/Product_page/product-m.htm).

Memory

- X5DL8-GG: Eight 184-pin DIMM sockets supporting up to 16 GB of registered ECC DDR-266/200 (PC2100/1600) SDRAM
- X5DLR-8G2+/X5DLR-8G2: Six 184-pin DIMM sockets supporting up to 12 GB of registered ECC DDR-266/200 (PC2100/1600) SDRAM

Note: Memory is 2-way interleaved meaning DIMM modules must be installed two at a time.

Chipset

- ServerWorks Grand Champion LE

Expansion Slots

- X5DL8-GG
  One 64-bit 133 MHz
  Five 64-bit 100 MHz PCI-X
- X5DLR-8G2+/X5DLR-8G2
  One 64-bit 133 MHz

Note: These are the default settings. Most PCI slots share a bus, which may impose speed limitations. See the PCI-X Bus Speed jumper setting in Chapter 2 for details.

BIOS

- 4 Mb AMI® Flash ROM

PC Health Monitoring

- Onboard voltage monitors for 2 CPU cores, chipset voltage, +5V, +12V, +3.3V and 5V standby
- Fan status monitor with firmware/software on/off control
- Environmental temperature monitor and control
- CPU fan auto-off in sleep mode
- Power-up mode control for recovery from AC power loss
- System overheat LED and control
- System resource alert
- IPMI 1.5 compliant (IPMI socket on board, daughter card required, X5DL8-GG only)

ACPI Features

- Microsoft OnNow
- Slow blinking LED for suspend state indicator
- Main switch override mechanism
- External modem ring-on

Onboard I/O

- AIC-7902 for dual channel Ultra320 SCSI
- Adaptec 2010S SCSI RAID support (X5DL8-GG)
- Adaptec 2015S SCSI RAID support (X5DLR-8G2+/X5DLR-8G2)
- Integrated ATI Rage XL Graphics Controller
- Intel 82540EM Gb Ethernet controller (X5DL8-GG - LAN1)
- Broadcom BCM5703 Gb Ethernet controller (X5DL8-GG - LAN2)
- Broadcom BCM5704 dual Gb Ethernet controller (X5DLR-8G2+/X5DLR-8G2)
- 2 EIDE bus master interfaces support Ultra DMA/100
- 1 floppy port interface (up to 2.88 MB)
- 2 Fast UART 16550A compatible serial ports
- 1 EPP/ECP (Enhanced Parallel Port/Extended Capabilities Port, not on X5DLR-8G2)
- PS/2 mouse and PS/2 keyboard ports
- 4 USB (Universal Serial Bus) ports (USB 1.1)

Other

- Internal/external modem ring-on
- Recovery from AC power loss control
- Wake-on-LAN (WOL)
- Console redirection
- APM 1.2, DMI 2.1, PCI 2.2, ACPI 1.0, Plug and Play (PnP), SMBIOS 2.3

CD/Diskette Utilities

- BIOS flash upgrade utility
- Device Drivers

Dimensions

- Extended ATX: 12.05" x 13" (306 x 330 mm)

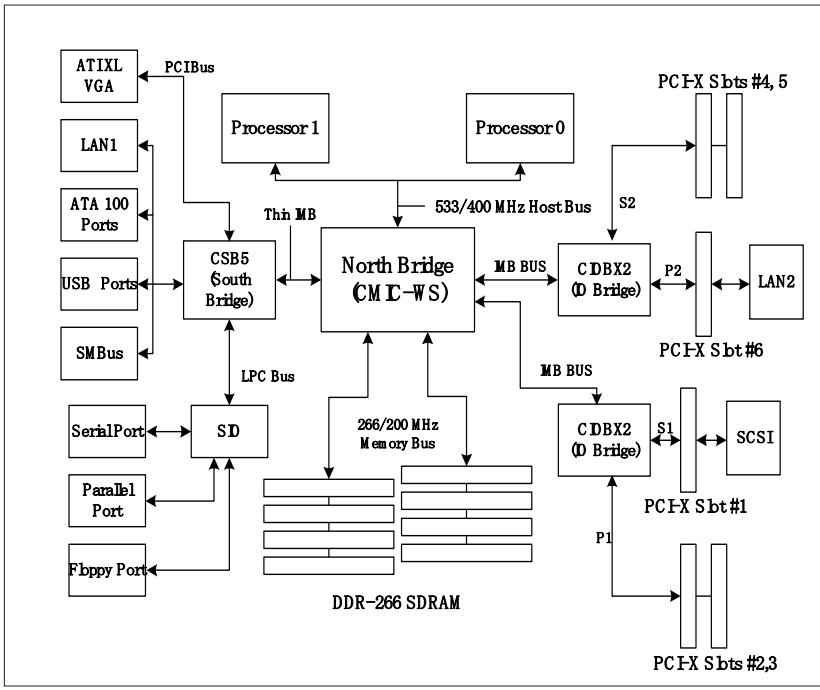


Figure 1-5. ServerWorks Grand Champion LE Chipset: System Block Diagram

Note: This is a general block diagram. Please see the previous Motherboard Features Section for details.

1-2 Chipset Overview

The ServerWorks Grand Champion LE™ is a high-performance work station SystemSet core logic chipset that consists of a North Bridge, a South Bridge and an IO bridge.

The North Bridge interfaces directly to the processor bus and integrates the functions of the main memory subsystem and the IMB bus interface unit. The memory subsystem consists of an 8-DIMM configuration accessed over a 144-bit memory bus (most chipsets have a 72-bit memory bus), which provides a significant boost in performance.

The South Bridge provides various integrated functions, including the PCI to ISA bridge and support for UDMA100, security (passwords and system protection), Plug & Play, USBs, power management, interrupt controllers and the SMBus.

The CIOBX2 is an integrated IO bridge that provides high-performance data flow between the IMB interface and the dual peer PCI-X bus interfaces. The X5DL8-GG has two CIOBX2 bridges (four buses).

1-3 Special Features

ATI Graphics Controller

The X5DL8-GG/X5DLR-8G2+/X5DLR-8G2 has an integrated ATI video controller based on the Rage XL graphics chip. The Rage XL fully supports sideband addressing and AGP texturing. This onboard graphics package can provide a bandwidth of up to 512 MB/sec over a 32-bit graphics memory bus.

BIOS Recovery

The BIOS Recovery function allows you to recover your BIOS image file if the BIOS flashing procedure fails (see Section 3-3).

Recovery from AC Power Loss

BIOS provides a setting for you to determine how the system will respond when AC power is lost and then restored to the system. You can choose for the system to remain powered off (in which case you must hit the power switch to turn it back on) or for it to automatically return to a power

on state. See the Power Lost Control setting in the Advanced BIOS Setup section (Peripheral Device Configuration) to change this setting. The default setting is Always On.

1-4 PC Health Monitoring

This section describes the PC health monitoring features of the SUPER X5DL8-GG/X5DLR-8G2+/X5DLR-8G2. It has an onboard System Hardware Monitor chip that supports PC health monitoring.

Onboard Voltage Monitors for the CPU Cores, Chipset Voltage, +5V, +12V and 5V Standby

An onboard voltage monitor will scan these voltages continuously. Once a voltage becomes unstable, a warning is given or an error message is sent to the screen. Users can adjust the voltage thresholds to define the sensitivity of the voltage monitor.

Fan Status Monitor with Firmware/Software On/Off Control

The PC health monitor can check the RPM status (tachometer reading) of the cooling fans. The onboard 3-pin CPU and chassis fans are controlled by the power management functions. The thermal fan is controlled by the overheat detection logic.

Environmental Temperature Control

The thermal control sensor monitors the CPU temperature in real time and will turn on the thermal control fan whenever the CPU temperature exceeds a user-defined threshold. The overheat circuitry runs independently from the CPU. It can continue to monitor for overheat conditions even when the CPU is in sleep mode. Once it detects that the CPU temperature is too high, it will automatically turn on the thermal control fan to prevent any overheat damage to the CPU. The onboard chassis thermal circuitry can monitor the overall system temperature and alert users when the chassis temperature is too high.

CPU Fan Auto-Off in Sleep Mode

The CPU fan activates when the power is turned on. It can be turned off when the CPU is in sleep mode. When in sleep mode, the CPU will not run at full power, thereby generating less heat.

System Resource Alert

This feature is available when used with Intel's LANDesk Client Manager (optional). LDCM is used to notify the user of certain system events. For example, if the system is running low on virtual memory and there is insufficient hard drive space for saving the data, you can be alerted of the potential problem.

Hardware BIOS Virus Protection

The system BIOS is protected by hardware that prevents viruses from infecting the BIOS area. The user can only change the BIOS content through the flash utility provided by Supermicro. This feature can prevent viruses from infecting the BIOS area and destroying valuable data.

Auto-Switching Voltage Regulator for the CPU Core

The auto-switching voltage regulator for the CPU core can support up to 20A current and auto-sense voltage IDs ranging from 1.4V to 3.5V. This will allow the regulator to run cooler and thus make the system more stable.

1-5 ACPI Features

ACPI stands for Advanced Configuration and Power Interface. The ACPI specification defines a flexible and abstract hardware interface that provides a standard way to integrate power management features throughout a PC system, including its hardware, operating system and application software. This enables the system to automatically turn on and off peripherals such as CD-ROMs, network cards, hard disk drives and printers. This also includes consumer devices connected to the PC such as VCRs, TVs, telephones and stereos.

In addition to enabling operating system-directed power management, ACPI provides a generic system event mechanism for Plug and Play and an operating system-independent interface for configuration control. ACPI leverages the Plug and Play BIOS data structures while providing a processor architecture-independent implementation that is compatible with both Windows 2000 and Windows NT 5.0.

Microsoft OnNow

The OnNow design initiative is a comprehensive, system-wide approach to system and device power control. OnNow is a term for a PC that is always on but appears to be off and responds immediately to user or other requests.

Slow Blinking LED for Suspend-State Indicator

When the CPU goes into a suspend state, the chassis power LED will start blinking to indicate that the CPU is in suspend mode. When the user presses any key, the CPU will wake-up and the LED will automatically stop blinking and remain on.

Main Switch Override Mechanism

When an ATX power supply is used, the power button can function as a system suspend button to make the system enter a SoftOff state. The monitor will be suspended and the hard drive will spin down. Depressing the power button again will cause the whole system to wake-up. During the SoftOff state, the ATX power supply provides power to keep the required circuitry in the system alive. In case the system malfunctions and you want to turn off the power, just depress and hold the power button for 4 seconds. This option can be set in the Power section of the BIOS Setup routine.

External Modem Ring-On

Wake-up events can be triggered by a device such as the external modem ringing when the system is in the SoftOff state. Note that external modem ring-on can only be used with an ATX 2.01 (or above) compliant power supply.

Wake-On-LAN (WOL)

Wake-On-LAN is defined as the ability of a management application to remotely power up a computer that is powered off. Remote PC setup, updates and asset tracking can occur after hours and on weekends so that daily LAN traffic is kept to a minimum and users are not interrupted. The motherboards have a 3-pin header (WOL) to connect to the 3-pin header on a Network Interface Card (NIC) that has WOL capability. Note that Wake-On-LAN can only be used with an ATX 2.01 (or above) compliant power

supply.

1-6 Power Supply

As with all computer products, a stable power source is necessary for proper and reliable operation. It is even more important for processors that have high CPU clock rates.

The SUPER X5DL8-GG/X5DLR-8G2+/X5DLR-8G2 accommodates ATX power supplies. Although most power supplies generally meet the specifications required by the CPU, some are inadequate. You should use one that will supply at least 400W of power - an even higher wattage power supply is recommended for high-load configurations. Also your power supply must provide a +5V standby voltage that supplies at least 720 mA of current. In addition, 1.5A is needed for LAN1 and LAN2.

NOTE: Auxiliary 12v power (Processor Power) is necessary to support Intel Xeon CPUs. Failure to provide this extra power will result in the CPUs becoming unstable after only a few minutes of operation. See Section 2-5 for details on connecting the power supply cables.

It is strongly recommended that you use a high quality power supply that meets ATX power supply Specification 2.02 or above. Additionally, in areas where noisy power transmission is present, you may choose to install a line filter to shield the computer from noise. It is recommended that you also install a power surge protector to help avoid problems caused by power surges.

1-7 Super I/O

The disk drive adapter functions of the Super I/O chip include a floppy disk drive controller that is compatible with industry standard 82077/765, a data separator, write pre-compensation circuitry, decode logic, data rate selection, a clock generator, drive interface control logic and interrupt and DMA logic. The wide range of functions integrated onto the Super I/O greatly reduces the number of components required for interfacing with floppy disk drives. The Super I/O supports 360 K, 720 K, 1.2 M, 1.44 M or 2.88 M disk drives and data transfer rates of 250 Kb/s, 500 Kb/s or 1 Mb/s.It also provides two high-speed, 16550 compatible serial communication ports (UARTs), one of which supports serial infrared communication. Each UART includes a 16-byte send/receive FIFO, a programmable baud rate generator,

complete modem control capability and a processor interrupt system.

Each UART includes a 16-byte send/receive FIFO, a programmable baud rate generator, complete modem control capability and a processor interrupt system. Both UARTs provide legacy speed with baud rate of up to 115.2 Kbps as well as an advanced speed with baud rates of 250 K, 500 K, or 1 Mb/s, which support higher speed modems.

The Super I/O supports one PC-compatible printer port (SPP), Bi-directional Printer Port (BPP) , Enhanced Parallel Port (EPP) or Extended Capabilities Port (ECP).

The Super I/O provides functions that comply with ACPI (Advanced Configuration and Power Interface), which includes support of legacy and ACPI power management through an SMI or SCI function pin. It also features auto power management to reduce power consumption.

The IRQs, DMAs and I/O space resources of the Super I/O can flexibly adjust to meet ISA PnP requirements, which suppport ACPI and APM (Advanced Power Management).

Chapter 2
Installation

2-1 Static-Sensitive Devices

Electric-Static-Discharge (ESD) can damage electronic components. To prevent damage to your system board, it is important to handle it very carefully. The following measures are generally sufficient to protect your equipment from ESD.

Precautions

- Use a grounded wrist strap designed to prevent static discharge.
- Touch a grounded metal object before removing the board from the antistatic bag.
- Handle the board by its edges only; do not touch its components, peripheral chips, memory modules or gold contacts.
- When handling chips or modules, avoid touching their pins.
- Put the motherboard and peripherals back into their antistatic bags when not in use.
- For grounding purposes, make sure your computer chassis provides excellent conductivity between the power supply, the case, the mounting fasteners and the motherboard.

Unpacking

The motherboard is shipped in antistatic packaging to avoid static damage. When unpacking the board, make sure the person handling it is static protected.

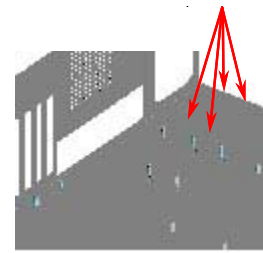
2-2 PGA Processor and Heatsink Installation

When handling the processor package, avoid placing direct pressure on the label area of the fan. Also, do not place the motherboard on a conductive surface, which can damage the BIOS battery and prevent the system from booting up.

IMPORTANT: Always connect the power cord last and always remove it before adding, removing or changing any hardware components. Make sure that you install the processor into the CPU socket **before** you install the CPU heat sink. Note: pictures show 603-pin socket.

1. Locate the following components, which are included in the shipping package.

*These screws are for mounting the motherboard to the back panel of a chassis that has four mounting holes (as shown on right).



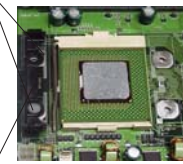
For chassis that do not have four mounting holes, use the anchor/peg assemblies:

Anchor/peg assemblies

2. Insert the white pegs into the black anchors. Do not force the white pegs all the way in - only about 1/3 of the way into the black anchors.

3. Place a retention bracket in the proper position and secure it by pressing pegs into two of the retention holes until you hear a *click*. The clicking sound indicates that the peg is locked and secured.

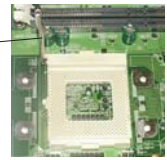
Two pegs in position



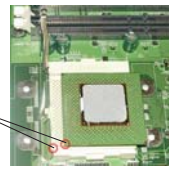
One retention bracket in position

4. Secure the other retention bracket into position by repeating Step 3.

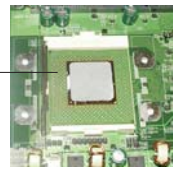
5. Lift the lever on the CPU socket: *lift the the lever completely or you will damage the CPU socket when power is applied*. *(Install CPU1 first.)*



6. Install the CPU in the socket. Make sure that pin 1 of the CPU is seated on pin 1 of the socket (both corners are marked with a triangle). When using only one CPU, install it into CPU socket #1 (CPU socket #2 is automatically disabled if only one CPU is used).



7. Press the lever down until you hear it *click* into the locked position.

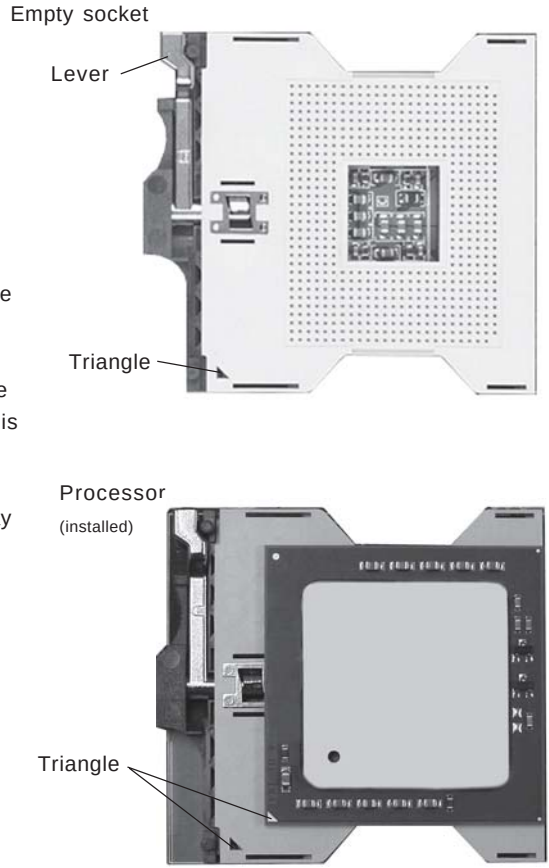


8. Apply the proper amount of thermal glue to the CPU die and place the heatsink and fan on top of the CPU.

9. Secure the heatsink by locking the retention clips into their proper position.

10. Connect the three wires of the CPU fan to the respective CPU fan connector.

Figure 2-1. PGA604 Socket: Empty and with Processor Installed



Warning! Make sure you lift the lever completely when installing the CPU. If the lever is only partly raised, damage to the socket or CPU may result.

Mounting the Motherboard in the Chassis

All motherboards have standard mounting holes to fit different types of chassis. Make sure the location of all the mounting holes for both the motherboard and the chassis match. Although a chassis may have both plastic and metal mounting fasteners, metal ones are highly recommended because they ground the motherboard to the chassis. Make sure the metal standoffs click in or are screwed in tightly. Then use a screwdriver to secure the motherboard onto the motherboard tray.

2-3 Installing DIMMs

Note: Check the Supermicro web site for recommended memory modules: http://www.supermicro.com/TECHSUPPORT/FAQs/Memory_vendors.htm

CAUTION

Exercise extreme care when installing or removing DIMM modules to prevent any possible damage.

DIMM Installation (See Figure 2-2)

1. Insert an even number of memory modules. *Interleaved memory requires you to install two modules at a time. With the X5DL8-GG, begin from the two slots of the **last** bank and working your way toward the two slots of Bank 1. With the X5DLR-8G2+/X5DLR-8G2, you may begin populating the slots two at a time (a full bank) from either end.*
2. Insert each DIMM module into its slot. Note the notch at the bottom of the module to prevent inserting the module incorrectly.
3. Gently press down on the DIMM module until it snaps into place in the slot. Repeat for all modules (see step 1 above).

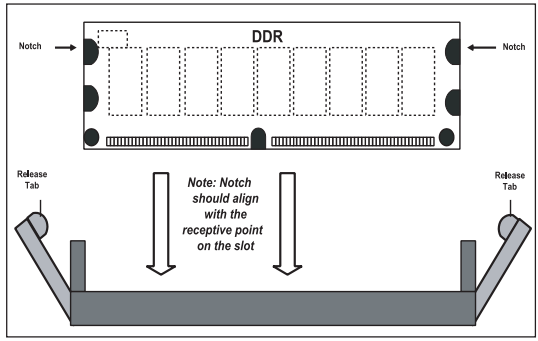
Support

The X5DL8-GG/X5DLR-8G2+/X5DLR-8G2 supports ECC registered DDR-266/200 (PC2100/1600) SDRAM memory. An interleaved memory configuration is used (see step 1 above).

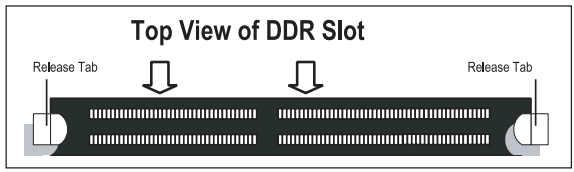
The interleaved memory scheme also employs an additional performance-enhancing feature. This feature works best when four DIMM slots are populated, is slightly reduced when all eight slots are populated, and is reduced slightly more with a two-slot configuration. In a six-slot configuration, this performance enhancing feature is not utilized, resulting in standard interleaved memory performance.

Figure 2-2. Installing and Removing DIMMs

To Install:
Insert the module vertically and press down until it snaps into place. Pay attention to the notch on the bottom of the module.



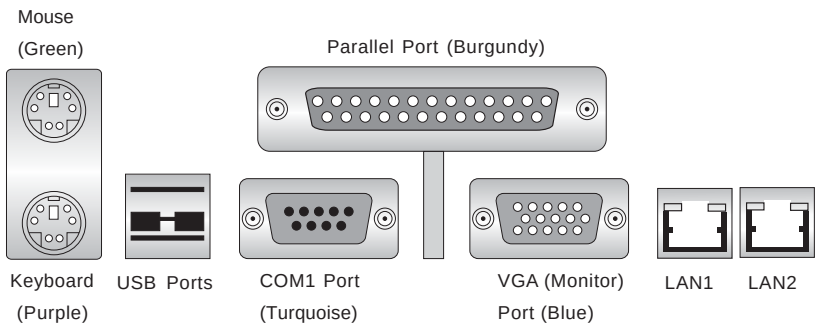
To Remove:
Use your thumbs to gently push near the edge of both ends of the module. This should release it from the slot.



2-4 IOPorts/Control Panel Connectors

The IO ports are color coded in conformance with the PC 99 specification. See Figure 2-3 below for the colors and locations of the various IO ports.

Figure 2-3. IO Port Locations and Definitions

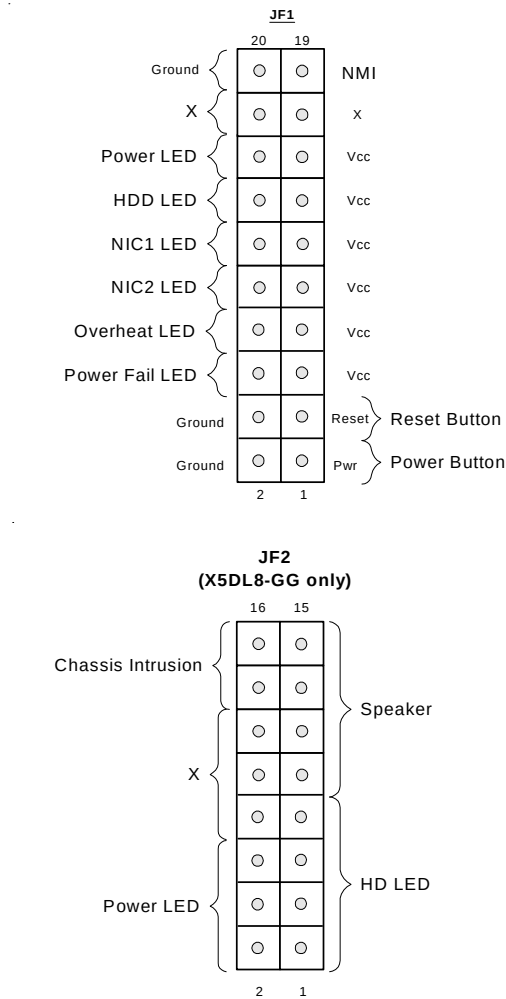


Note: COM2 is a header on the motherboard (see motherboard layout for location). The X5DLR-8G2+/X5DLR-8G2 does not have a parallel port.

Front Control Panel

JF1 contains header pins for various front control panel connectors. These connectors are designed for use with Supermicro server chassis. See Figure 2-4 for the pin locations of the various front control panel buttons and LED indicators. Refer to the following section for descriptions and pin definitions. JF2 is an additional row of headers that provides connectors for additional functions, as noted below.

Figure 2-4. JF1/JF2 Header Pins



2-5 Connecting Cables

ATX Power Connector

The power supply connector meets the SSI (Superset ATX) 24-pin specification, however it also supports a 20-pin power supply connector. Make sure that the orientation of the PS connector is correct. See the table on the right for pin definitions.

ATX Power Supply 24-pin Connector Pin Definitions

Pin Number	Definition	Pin Number	Definition
13	+3.3V	1	+3.3V
14	-12V	2	+3.3V
15	COM	3	COM
16	PS_ON#	4	+5V
17	COM	5	COM
18	COM	6	+5V
19	COM	7	COM
20	Res(NC)	8	PWR_OK
21	+5V	9	5VSB
22	+5V	10	+12V
23	+5V	11	+12V
24	COM	12	+3.3V

Processor Power Connector

In addition to the Primary ATX power connector (above), the 12v 8-pin Processor Power Connector must also be connected to your power supply. See the table on the right for pin definitions.

8-Pin +12v Processor Power Connector (J56)

Pins	Definition
1 thru 4	Ground
5 thru 8	+12v

NMI Button

The non-maskable interrupt button header is located on pins 19 and 20 of JF1. Refer to the table on the right for pin definitions.

NMI Button Pin Definitions (JF2)

Pin Number	Definition
19	Control
20	Ground

Power LED

The Power LED connection is located on pins 15 and 16 of JF1. Refer to the table on the right for pin definitions.

PWR_LED Pin Definitions (JF1)

Pin Number	Definition
15	+5V
16	Control

HDD LED

The HDD LED (for IDE and SCSI disk drives) connection is located on pins 13 and 14 of JF1. Attach the IDE hard drive LED cable to these pins to display disk activity. Refer to the table on the right for pin definitions.

(IDE) HDD LED Pin Definitions (JF1)

Pin Number	Definition
13	+5V
14	HD Active

NIC1 LED

The NIC1 (LAN1) LED connection is located on pins 11 and 12 of JF1. Attach the NIC1 LED cable to display network activity. Refer to the table on the right for pin definitions.

NIC/LAN1 LED Pin Definitions (JF1)

Pin Number	Definition
11	+5V
12	GND

NIC2 LED

The NIC2 (LAN2) LED connection is located on pins 9 and 10 of JF1. Attach the NIC2 LED cable to display network activity. Refer to the table on the right for pin definitions.

NIC/LAN2 LED Pin Definitions (JF1)

Pin Number	Definition
9	+5V
10	GND

Overheat LED (OH)

Connect an LED to the OH connection on pins 7 and 8 of JF1 to provide advanced warning of chassis overheating. Refer to the table on the right for pin definitions.

Overheat (OH) LED Pin Definitions (JF1)

Pin Number	Definition
7	+5V
8	GND

Power Fail LED

The Power Fail LED connection is located on pins 5 and 6 of JF1. Refer to the table on the right for pin definitions.

Power Fail LED Pin Definitions (JF1)

Pin Number	Definition
5	Control
6	GND

Reset

The Reset connection is located on pins 3 and 4 of JF1. Attach it to the hardware reset switch on the computer case. Refer to the table on the right for pin definitions.

Reset Pin Definitions (JF1)

Pin Number	Definition
3	Reset
4	Ground

PWR_ON

The PWR_ON connection is located on pins 1 and 2 of JF1. Momentarily contacting both pins will power on/off the system. This button can also be configured to function as a suspend button (see the Power Button Mode setting in BIOS). To turn off the power when set to suspend mode, depress the button for at least 4 seconds. Refer to the table on the right for pin definitions.

PWR_ON Connector Pin Definitions (JF1)

Pin Number	Definition
1	PW_ON
2	Ground

Universal Serial Bus (USB0/1)

Two Universal Serial Bus ports are located beside the keyboard/mouse ports. USB0 is the bottom connector and USB1 is the top connector. See the table on the right for pin definitions.

Universal Serial Bus Pin Definitions

USB0		USB1	
Pin Number	Definition	Pin Number	Definition
1	+5V	1	+5V
2	P0-	2	P0-
3	P0+	3	P0+
4	Ground	4	Ground
5	N/A	5	Key

Serial Ports

The COM1 serial port is located under the parallel port (see Figure 2-3). See the table on the right for pin definitions. See the motherboard layout diagrams for the location of the COM2 connector, which is a header.

Serial Port Pin Definitions (COM1, COM2)

Pin Number	Definition	Pin Number	Definition
1	CD	6	DSR
2	RD	7	RTS
3	TD	8	CTS
4	DTR	9	RI
5	Ground	10	NC

PS/2 Keyboard and Mouse Ports

The ATX PS/2 keyboard and the PS/2 mouse are located on J11. See the table on the right for pin definitions. (The mouse port is above the keyboard port. See Figure 2-3.)

PS/2 Keyboard and Mouse Port Pin Definitions (J11)

Pin Number	Definition
1	Data
2	NC
3	Ground
4	VCC
5	Clock
6	NC

Fan Headers*

The motherboard has fan headers for CPU, chassis and overheat fans. See the table on the right for pin definitions.

Fan Header Pin Definitions (CPU/CHS/OH Fans)

Pin Number	Definition
1	Ground (black)
2	+12V (red)
3	Tachometer

Caution: These fan headers are DC power.

GLAN1/GLAN2 Ethernet Ports

Two gigabit Ethernet ports are located beside the VGA port on the IO backplane. These ports accept RJ45 type cables. See the next section for a description of the LEDs on the LAN ports.

HD LED Indicator (JF2)

The HD LED connector located at JF2 is used to indicate activity on any hard drive (IDE, SCSI or CD-ROM).

Power LED (JF2)

The Power LED connection located at JF2 is used to inform you that power is being supplied to the motherboard. There is also an onboard LED for this function (see CR5 in Section 2-6).

Speaker (X5DL8-GG)

A speaker header/jumper is located on JF2. You may enable the onboard speaker by jumping pins 13 & 15 of JF2. To use an external speaker, connect the speaker header to pins 9 through 15.

Third Power Supply Fail Header

Connect a cable from your power supply to the JP46 header to provide warning of power supply failure. The warning signal is passed through the PWR_LED pin on JF1 to provide indication of a power failure on the chassis. **Note:** This feature is only available when using Supermicro power supplies. See the table on the right for pin definitions.

Third Power Supply Fail Header Pin Definitions (JP46)

Pin Number	Definition
1	P/S 1 Fail Signal
2	P/S 2 Fail Signal
3	P/S 3 Fail Signal
4	Reset (from MB)

Wake-On-LAN (X5DL8-GG)

The Wake-On-LAN header is designated as WOL. See the table on the right for pin definitions. You must have a LAN card with a Wake-on-LAN connector and cable to use this feature.

Wake-On-LAN Pin Definitions (WOL)

Pin Number	Definition
1	+5V Standby
2	Ground
3	Wake-up

Chassis Intrusion

A Chassis Intrusion header is located at JP57. Attach the correct connector here to inform you of a chassis intrusion condition.

Extra Universal Serial Bus Headers (USB2/3)

Two USB headers are located at J1. The odd numbered pins are for USB2 and the even numbered pins at the edge of the board) are for USB3. A USB cable (not included) is needed for use. See the tables on the right.

USB2 Pin Definitions (J1)

Pin Number	Definition
1	Power
3	-
5	+
7	Ground

USB3 Pin Definitions (J1)

Pin Number	Definition
2	Power
4	-
6	+
8	Ground

IPMB (X5DL8-GG)

An IPMB (IPMI Bus) header is located at J20 to support IPMI, a server management standard. Connect the appropriate cable from the IPMI daughter board to J20 to utilize IPMI on your system.

IPMB Header Pin Definitions (J20)

Pin Number	Definition
1	Data
2	Ground
3	Clock
4	No Connection

SMB

A System Management Bus header is located at J21. Connect the appropriate cable here to utilize SMB on your system.

SMB Header Pin Definitions (J21)

Pin Number	Definition
1	Data
2	Ground
3	Clock
4	No Connection

2-6 Onboard Indicators

GLAN1/GLAN2 LEDs

Each of the Ethernet ports (located beside the VGA port) has a yellow and a green LED. See the tables below for the functions associated with these LEDs. On each Gb LAN port, the yellow LED indicates activity while the other LED may be green, orange or off to indicate the speed of the connection (as specified in the tables below).

Gb LAN Left LED Indicator

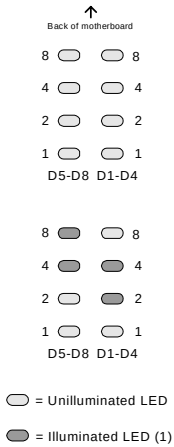
LED Color	Definition
Off	Not Active
Yellow	Active

Gb LAN Right LED Indicator

LED Color	Definition
Off	No Connection
Green	100 MHz
Orange	1 GHz

Debug LEDs

Two sets of surface-mounted debug LEDs are located beside the LAN2 port and are each composed of four individual LEDs (D1 through D8) , which are used to provide POST code information. See the diagrams below for reading the debug LEDs and refer to Appendix B for a complete list of POST codes (a partial listing of the most common codes are given below).



Reading the Debug LEDs:
When on, each of the eight separate LEDs represent the value of the number shown beside it in the diagram. Add up the numerical values of each illuminated LED in the D5-D8 row to get the high digit (left) and those in the D1-D4 row to get the low (right) digit of the corresponding hexidecimal POST code.

Example:
The example on the left indicates a hexidecimal POST code of C6. This is determined in the following manner:
D1-D4 (right digit): 4 + 2 = 6
D5-D8 (left digit): 8 + 4 = 12
(decimal 12 = hexidecimal C)

Decimal	Hexidecimal Equivalent
0-9	0-9
10	A
11	B
12	C
13	D
14	E
15	F

Common POST Codes:
The following is a list of the most common POST codes that you may see.

POST Code	Meaning
01	Displayed while in BIOS Setup
31	No video card
40	Displayed while counting memory
83	Displayed when memory count is finished
85	CMOS Clear
95	Displayed while detecting IDE devices
DE	No memory
DE	Wrong type of memory installed
DE	One memory module (two minimum required)

CR5 LED

CR5 is an onboard LED that serves as a power indicator. See the table on the right for the meaning of each of the three colors displayed by CR5.

Onboard LED Power Indicator (CR5)

LED Color	Definition
Green	Power On
Yellow	Standby Mode
Red	Wrong CPU

2-7 DIP Switch Settings

DIP Switch 4: Processor Speed

The red "DIP" switch labeled SW4 has four individual switches, which are used to set the speed of the processor.

The table on the right shows you the switch settings for the various speeds your processor may be able to run at. (This table is also silkscreened on the motherboard.)

Note: Most Intel processors have a fixed Core/Bus ratio that overwrites the setting of DIP Switch 4. In most cases you *do not* need to make any changes to SW4.

Processor Speed Selection (DIP Switch 4)

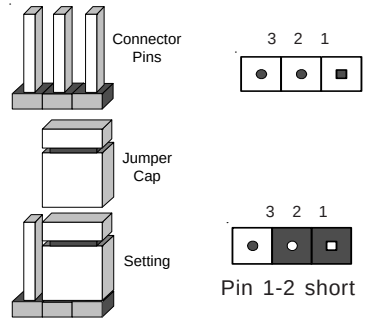
CPU	SW #1	SW #2	SW #3	SW #4
1.3 GHz	ON		ON	
1.4 GHz		ON	ON	
1.5 GHz	ON	ON	ON	
1.6 GHz				ON
1.7 GHz	ON			ON
1.8 GHz		ON		ON
1.9 GHz	ON	ON		ON
2.0 GHz			ON	ON
2.1 GHz	ON		ON	ON
2.2 GHz		ON	ON	ON
2.4 GHz	ON	ON	ON	ON

2-8 Jumper Settings

Explanation of Jumpers

To modify the operation of the motherboard, jumpers can be used to choose between optional settings. Jumpers create shorts between two pins to change the function of the connector. Pin 1 is identified with a square solder pad on the printed circuit board. See the motherboard layout pages for jumper locations.

Note: On two pin jumpers, "Closed" means the jumper is on and "Open" means the jumper is off the pins.



CMOS Clear

JBT1 is used to clear CMOS (which will also clear any passwords). Instead of pins, this jumper consists of contact pads to prevent accidentally clearing the contents of CMOS.

To clear CMOS, first power down the system, then

1) Unplug the power cord(s)

2) With the power disconnected, short the CMOS pads with a metal object such as a small screwdriver

3) Remove the screwdriver (or shorting device)

4) Reconnect the power cord(s) and power on the system.

Note: *Do not use the PW_ON connector to clear CMOS*.

SpeakerEnable/Disable (X5DL8-GG)

To enable use of the onboard speaker, put a jumper on pins 13 and 15 of JF2. Removing the jumper will disable the onboard speaker.

SpeakerEnable/Disable (X5DLR-8G2+, X5DLR-8G2)

To disable the onboard speaker, remove the jumper from JP2 (see the table on the right).

Speaker Enable/Disable Jumper Settings (JP2)

Jumper Position	Definition
Closed	Enabled
Open	Disabled

Fan Detection Select

JP58 allows you to select which fan speed to have displayed in the Hardware Monitors section of BIOS (the CPU1/2 fans or the CPU1/CPU2 Chassis fans). The default position is open to select the CPU1/2 fans. See the table on the right for jumper settings.

Fan Detection Select Jumper Settings (JP58)

Jumper Position	Definition
Open	CPU1/2 Fans
Closed	CPU1/2 Ch Fans

Chassis/Overheat Fan Select

JP48 allows you to select to use either the chassis fan or the overheat fan. The default position is closed to select the chassis fan. See the table on the right for jumper settings.

Chassis/Overheat Fan Select Jumper Settings (JP48)

Jumper Position	Definition
Open	Overheat Fan
Closed	Chassis Fan

Watch Dog

JP3 controls the Watch Dog function. Watch Dog is a system monitor that takes action when a software application freezes the system. Pins 1-2 will have WD reset the system if a program freezes. Pins 2-3 will generate a non-maskable interrupt for the program that has frozen (requires software implementation). See the table on the right for jumper settings. Watch Dog must also be enabled in BIOS.

Watch Dog Jumper Settings (JP3)

Jumper Position	Definition
Pins 1-2	WD to Reset
Pins 2-3	WD to NMI
Open	Disabled

GLAN1 Enable/Disable (X5DL8-GG)

Change the setting of jumper JP54 to enable or disable the onboard LAN1 port on the motherboard. See the table on the right for jumper settings. The default setting is pins 1-2.

LAN1 Enable/Disable Jumper Settings (JP54)

Jumper Position	Definition
Pins 1-2	Enabled
Pins 2-3	Disabled

GLAN2 Enable/Disable (X5DL8-GG)

Change the setting of jumper JP4 to enable or disable the onboard LAN2 port on the motherboard. See the table on the right for jumper settings. The default setting is pins 1-2.

LAN2 Enable/Disable Jumper Settings (JP4)

Jumper Position	Definition
Pins 1-2	Enabled
Pins 2-3	Disabled

SCSI Enable/Disable

The SCSI Enable/Disable jumper at JA4 allows you to enable or disable the onboard SCSI. The normal (default) position is on pins 1-2 to enable SCSI. See the table on the right for jumper settings.

SCSI Enable/Disable Jumper Settings (JA4)

Jumper Position	Definition
Pins 1-2	Enabled
Pins 2-3	Disabled

SCSI Termination Enable/ Disable

Jumpers JPA1 and JPA2 allow you to enable or disable termination for the SCSI connectors. Jumper JPA1 controls SCSI channel A and JPA2 is for SCSI channel B. The default setting is open to enable (teminate) both SCSI channels. See the table on the right for jumper settings.

SCSI Channel Termination Enable/Disable Jumper Settings (JPA1, JPA2)

Jumper Position	Definition
Open	Enabled
Closed	Disabled

PCI-X Bus Speed Setting (X5DL8-GG)

Jumpers P1, P2, S1 and S2 are used to change the speeds for the four PCI-X buses. See the table on the right for jumper settings.

PCI-X Buses:

S1: Bus for PCI-X slot #1 and SCSI
P1: Bus for PCI-X slots #2 and #3
S2: Bus for PCI-X slots #4 and #5
P2: Bus for PCI-X slot #6 and LAN2

Note: If two cards are used in slots that share a bus, both slots will run at 100 MHz (maximum).

PCI-X Slot Bus Speed Settings
Pin Definitions
(P1, P2, S1, S2)

Pin Setting	Speed
Pins 1-2	PCI 33/66 MHz
Pins 2-3	PCI-X 66 MHz
Pins 3-4	PCI-X 100 MHz
Pins 4-5	PCI-X 133 MHz

Default setting is PCI-X 100 MHz for all slots.

PCI-X Bus Speed Setting (X5DLR-8G2+, X5DLR-8G2)

Jumper P2 is used to change the speed of the single PCI-X bus on the motherboard. See the table on the right for jumper settings.

Note: The PCI-X bus is also tied to the SCSI controller. If using a 33/66 MHz PCI card in this slot, you will slow the SCSI speed down to 33 or 66 MHz.

PCI-X Slot Bus Speed Settings
Pin Definitions
(P2)

Pin Setting	Speed
Pins 1-2	PCI 33/66 MHz
Pins 2-3	PCI-X 66 MHz
Pins 3-4	PCI-X 100 MHz
Pins 4-5	PCI-X 133 MHz

This slot was designed for use with PCI-X cards - some PCI cards may work in the slot.

33 MHz PCI Enable/Disable (X5DL8-GG)

If you wish to use 33 MHz PCI cards, close J29 to force the P1 bus (slots 2 & 3) to run at 33 MHz. See the table on the right for jumper settings.

Note: if you force the slots(s) to 33 MHz, you must set the P1 bus speed jumpers (above) to the lowest speed.

33 MHz PCI
Enable/Disable
Jumper Settings
(J29)

Jumper Position	Definition
Open	Normal
Closed	33 MHz PCI

Front Side Bus Speed

JP12 is used to set the system (front side) bus speed for the processors. It is best to keep this jumper set to Auto. See the table on the right for jumper settings.

Front Side Bus Speed Jumper Settings (JP12)

Jumper Position	Definition
Pins 1-2	Auto
Pins 2-3	400 MHz
Open	533 Mhz

Spread Spectrum

J35 is used to enable or disable the Spread Spectrum feature. Spread Spectrum is a technique used to stabilize operations when a system is being affected by electromagnetic interference. The normal (default) position is open to disable Spread Spectrum. See table at right for jumper settings.

Spread Spectrum Enable/Disable Jumper Settings (J35)

Jumper Position	Definition
Open	Disabled
Closed	Enabled

PCI 3.3V Standby Enable/ Disable (X5DL8-GG)

JP2 is used to enable or disable a 3.3V standby voltage on pin A14 of the PCI-X slots. If you have a LAN or modem add-on card inserted into a PCI-X slot that you wish to "wake" the system up with, you should enable this jumper. Otherwise, leave this jumper on pins 1-2 (disabled). The normal (default) position is disabled. See the table on the right for jumper settings.

PCI 3.3V Standby Enable/ Disable Jumper Settings (JP2)

Jumper Position	Definition
Pins 1-2	Disabled
Pins 2-3	Enabled

VGA Enable/Disable

JP56 allows you to enable or disable the VGA port. The default position is on pins 1 and 2 to enable VGA. See the table on the right for jumper settings.

VGA Enable/Disable Jumper Settings (JP56)

Jumper Position	Definition
1-2	Enabled
2-3	Disabled

Main Power Override (X5DL8-GG)

Instead of using the chassis power on switch, you may close jumper JP7 to apply power to the system. This effectively disables the power button from turning off the system. See the table on the right for jumper settings. The default setting is Open (normal).

Power On Jumper Settings (JP1)

Jumper Position	Definition
Open	Normal
Closed	Force Power On

2-9 Parallel Port, Floppy/Hard Disk Drive and SCSI Connections

Note the following when connecting the floppy and hard disk drive cables:

- The floppy disk drive cable has seven twisted wires.
- A red mark on a wire typically designates the location of pin 1.
- A single floppy disk drive ribbon cable has 34 wires and two connectors to provide for two floppy disk drives. The connector with twisted wires always connects to drive A, and the connector that does not have twisted wires always connects to drive B.

Parallel Port Connector

The parallel port is located on J65. See the table below right for pin definitions.

Parallel (Printer) Port Pin Definitions (J65)

Pin Number	Function	Pin Number	Function
1	Strobe-	2	Auto Feed-
3	Data Bit 0	4	Error-
5	Data Bit 1	6	Init-
7	Data Bit 2	8	SLCT IN-
9	Data Bit 3	10	GND
11	Data Bit 4	12	GND
13	Data Bit 5	14	GND
15	Data Bit 6	16	GND
17	Data Bit 7	18	GND
19	ACK	20	GND
21	BUSY	22	GND
23	PE	24	GND
25	SLCT	26	NC

Floppy Connector

The floppy connector is located on J12. See the table below for pin definitions.

Floppy Connector Pin Definitions (JP12)

Pin Number	Function	Pin Number	Function
1	GND	2	FDHDIN
3	GND	4	Reserved
5	Key	6	FDEDIN
7	GND	8	Index-
9	GND	10	Motor Enable
11	GND	12	Drive Select B-
13	GND	14	Drive Select A-
15	GND	16	Motor Enable
17	GND	18	DIR-
19	GND	20	STEP-
21	GND	22	Write Data-
23	GND	24	Write Gate-
25	GND	26	Track 00-
27	GND	28	Write Protect-
29	GND	30	Read Data-
31	GND	32	Side 1 Select-
33	GND	34	Diskette

IDE Connectors

There are no jumpers to configure the onboard IDE#1 and #2 connectors (J18 and J19, respectively). See the table on the right for pin definitions.

IDE Connector Pin Definitions (J18, J19)

Pin Number	Function	Pin Number	Function
1	Reset IDE	2	GND
3	Host Data 7	4	Host Data 8
5	Host Data 6	6	Host Data 9
7	Host Data 5	8	Host Data 10
9	Host Data 4	10	Host Data 11
11	Host Data 3	12	Host Data 12
13	Host Data 2	14	Host Data 13
15	Host Data 1	16	Host Data 14
17	Host Data 0	18	Host Data 15
19	GND	20	Key
21	DRQ3	22	GND
23	I/O Write-	24	GND
25	I/O Read-	26	GND
27	IOCHRDY	28	BALE
29	DACK3-	30	GND
31	IRQ14	32	IOCS16-
33	Addr 1	34	GND
35	Addr 0	36	Addr 2
37	Chip Select 0	38	Chip Select 1-
39	Activity	40	GND

Ultra320 SCSI Connector

Refer to the table below for the pin definitions of the Ultra320 SCSI connectors located at JA1 and JA2.

68-pin Ultra320 SCSI Connectors (JA1 and JA2)

Connector Contact Number	Signal Names	Connector Contact Number	Signal Names
1	+DB(12)	35	-DB(12)
2	+DB(13)	36	-DB(13)
3	+DB(14)	37	-DB(14)
4	+DB(15)	38	-DB(15)
5	+DB(P1)	39	-DB(P1)
6	+DB(0)	40	-DB(0)
7	+DB(1)	41	-DB(1)
8	+DB(2)	42	-DB(2)
9	+DB(3)	43	-DB(3)
10	+DB(4)	44	-DB(4)
11	+DB(5)	45	-DB(5)
12	+DB(6)	46	-DB(6)
13	+DB(7)	47	-DB(7)
14	+DB(P)	48	-DB(P)
15	GROUND	49	GROUND
16	DIFFSENS	50	GROUND
17	TERMPWR	51	TERMPWR
18	TERMPWR	52	TERMPWR
19	RESERVED	53	RESERVED
20	GROUND	54	GROUND
21	+ATN	55	-ATN
22	GROUND	56	GROUND
23	+BSY	57	-BSY
24	+ACK	58	-ACK
25	+RST	59	-RST
26	+MSG	60	-MSG
27	+SEL	61	-SEL
28	+C/D	62	-C/D
29	+REQ	63	-REQ
30	+I/O	64	-I/O
31	+DB(8)	65	-DB(8)
32	+DB(9)	66	-DB(9)
33	+DB(10)	67	-DB(10)
34	+DB(11)	68	-DB(11)

2-10 Installing Software Drivers

After all the hardware has been installed you must install the software drivers. The necessary drivers are all included on the Supermicro CD that came packaged with your motherboard. After inserting this CD into your CDROM drive, the display shown in Figure 2-5 should appear. (If this display does not appear, click on the My Computer icon and then on the icon representing your CDROM drive. Finally, double click on the S "Setup" icon.)

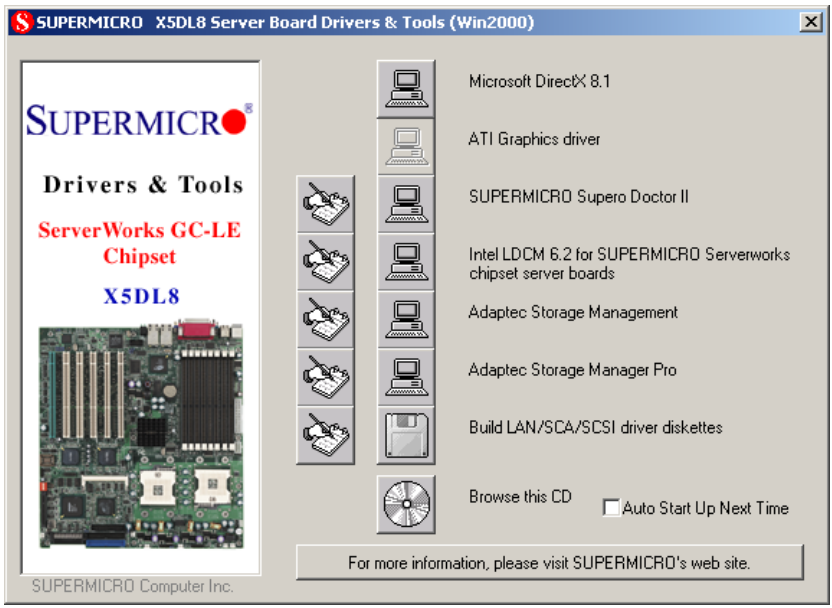


Figure 2-5. Driver/Tool Installation Display Screen

Click the icons showing a hand writing on paper to view the readme files for each item. The bottom icon with a CD on it allows you to view the entire contents of the CD.

Chapter 3
Troubleshooting

3-1 Troubleshooting Procedures

Use the following procedures to troubleshoot your system. If you have followed all of the procedures below and still need assistance, refer to the 'Technical Support Procedures' and/or 'Returning Merchandise for Service' section(s) in this chapter.

Note: Always disconnect the power cord before adding, changing or installing any hardware components.

Before Power On

1. Make sure no short circuits exist between the motherboard and chassis.
2. Disconnect all ribbon/wire cables from the motherboard, including those for the keyboard and mouse.
3. Remove all add-on cards.
4. Install one CPU (making sure it is fully seated) and connect the chassis speaker and the power LED to the motherboard. (Check all jumper settings as well.)

No Power

1. Make sure no short circuits exist between the motherboard and the chassis.
2. Verify that all jumpers are set to their default positions.
3. Check that the 115V/230V switch on the power supply is properly set.
4. Turn the power switch on and off to test the system.
5. The battery on your motherboard may be old. Check to verify that it still supplies ~3VDC. If it does not, replace it with a new one.

No Video

1. If the power is on but you have no video, remove all the add-on cards and cables.
2. Use the speaker to determine if any beep codes exist. Refer to Appendix A for details on beep codes.

NOTE

If you are a system integrator, VAR or OEM, a POST diagnostics card is recommended. For I/O port 80h codes, refer to App. B.

Memory Errors

1. Make sure the DIMM modules are properly and fully installed.
2. Determine if different speeds of DIMMs have been installed and verify that the BIOS setup is configured for the fastest speed of RAM used. It is recommended to use the same RAM speed for all DIMMs in the system.
3. Make sure you are using registered ECC, PC2100 or 1600 (DDR-266 or 200) SDRAM. EDO SDRAM and PC100/133 SDRAM are not supported.
4. Check for bad DIMM modules or slots by swapping a single module between two slots and noting the results.
5. Make sure all memory modules are fully seated in their slots.
6. Check the power supply voltage 115V/230V switch.

Losing the System's Setup Configuration

1. Ensure that you are using a high quality power supply. A poor quality power supply may cause the system to lose the CMOS setup information. Refer to Section 1-6 for details on recommended power supplies.
2. The battery on your motherboard may be old. Check to verify that it still supplies ~3VDC. If it does not, replace it with a new one.
3. If the above steps do not fix the Setup Configuration problem, contact your vendor for repairs.

3-2 Technical Support Procedures

Before contacting Technical Support, please take the following steps. Also, note that as a motherboard manufacturer, Super Micro does not sell directly to end-users, so it is best to first check with your distributor or reseller for troubleshooting services. They should know of any possible problem(s) with the specific system configuration that was sold to you.

1. Please go through the 'Troubleshooting Procedures' and 'Frequently Asked Question' (FAQ) sections in this chapter or see the FAQs on our web site (http://www.supermicro.com/techsupport.htm) before con-

tacting Technical Support.

2. BIOS upgrades can be downloaded from our web site at http://www.supermicro.com/TECHSUPPORT/BIOS/bios.htm.

Note: Not all BIOS can be flashed depending on the modifications to the boot block code.

3. If you still cannot resolve the problem, include the following information when contacting Super Micro for technical support:
   - Motherboard model and PCB revision number
   - BIOS release date/version (this can be seen on the initial display when your system first boots up)
   - System configuration

   An example of a Technical Support form is on our web site at http://www.supermicro.com/techsupport/contact_support.htm.
4. Distributors: For immediate assistance, please have your account number ready when placing a call to our technical support department. We can be reached by e-mail at support@supermicro.com, by fax at (408) 503-8019 or by phone at (408) 503-8000, option 2.

3-3 Frequently Asked Questions

Question: What are the various types of memory that the X5DL8-GG/X5DLR-8G2+/X5DLR-8G2 motherboard can support?

Answer: The X5DL8-GG has eight and the X5DLR-8G2+/X5DLR-8G2 has six 184-pin DIMM slots, which support registered ECC DDR-266 and DDR-200 (PC2100 and PC1600) DIMMs only. Unbuffered SDRAM, non-ECC memory and PC100/133 SDRAM modules are not supported. **Important:** The memory employs a two-way interleaved scheme, which requires you to install memory modules in pairs (see Chapter 2 Section 3 for details.)

Question: How do I update my BIOS?

Answer: It is recommended that you **do not** upgrade your BIOS if you are experiencing no problems with your system. Updated BIOS files are located on our web site at http://www.supermicro.com. Please check our BIOS warning message and the info on how to update your BIOS on our web site. Also, check the current BIOS revision and make sure it is newer than your BIOS before downloading. Select your motherboard model and download the BIOS file to your computer. Unzip the BIOS update file and you will

find the readme.txt (flash instructions), the flash.bat (BIOS flash utility) and the BIOS image (xxxxxx.rom) files. Copy these files onto a bootable floppy and reboot your system. It is not necessary to set BIOS boot block protection jumpers on the motherboard. At the DOS prompt, enter the command "flash." This will start the flash utility and give you an opportunity to save your current BIOS image. Flash the boot block and enter the name of the update BIOS image file.

Note: It is important to save your current BIOS and **rename it "super.rom"** in case you need to recover from a failed BIOS update. Select flash boot block, then enter the update BIOS image. Select "Y" to start the BIOS flash procedure and do not disturb your system until the flash utility displays that the procedure is complete. After updating your BIOS, please clear the CMOS then load Optimal Values in the BIOS.

Question: After flashing the BIOS my system does not have video. How can I correct this?

Answer: If the system does not have video after flashing your new BIOS, it indicates that the flashing procedure failed. To remedy this, first clear CMOS per the instructions in this manual and retry the BIOS flashing procedure. If you still do not have video, please use the following **BIOS Recovery Procedure**. First, turn your system off and place the floppy disk with the saved BIOS image file (see above FAQ) in drive A. Press and hold <CTRL> and <Home> at the same time, then turn on the power with these keys pressed until your floppy drive starts reading. Your screen will remain blank until the BIOS program is done. If the system reboots correctly, then the recovery was successful. The BIOS Recovery Procedure will not update the boot block in your BIOS.

Question: What's on the CD that came with my motherboard?

Answer: The supplied compact disc has quite a few drivers and programs that will greatly enhance your system. We recommend that you review the CD and install the applications you need. Applications on the CD include chipset drivers for Windows and security drivers.

Question: Why can't I turn off the power using the momentary power on/off switch?

Answer: The instant power off function is controlled in BIOS by the Power Button Mode setting. When the On/Off feature is enabled, the motherboard will have instant off capabilities as long as the BIOS has control of the system. When the Standby or Suspend feature is enabled or when the

BIOS is not in control such as during memory count (the first screen that appears when the system is turned on), the momentary on/off switch must be held for more than four seconds to shut down the system. This feature is required to implement the ACPI features on the motherboard.

3-4 Returning Merchandise for Service

A receipt or copy of your invoice marked with the date of purchase is required before any warranty service will be rendered. You can obtain service by calling your vendor for a Returned Merchandise Authorization (RMA) number. When returning to the manufacturer, the RMA number should be prominently displayed on the outside of the shipping carton, and mailed prepaid or hand-carried. Shipping and handling charges will be applied for all orders that must be mailed when service is complete.

This warranty only covers normal consumer use and does not cover damages incurred in shipping or from failure due to the alternation, misuse, abuse or improper maintenance of products.

During the warranty period, contact your distributor first for any product problems.

Notes

Chapter 4
AMIBIOS

4-1 Introduction

This chapter describes the AMIBIOS for the X5DL8-GG/X5DLR-8G2+/X5DLR-8G2. The AMI ROM BIOS is stored in a Flash EEPROM and can be easily upgraded using a floppy disk-based program.

Note: Due to periodic changes to BIOS, some settings may have been added or deleted and might not yet be recorded in this manual. Refer to the Manual Download area of our web site for any changes to BIOS that are not reflected in this manual.

System BIOS

The BIOS is the Basic Input Output System used in all IBM® PC, XT™, AT®, and PS/2® compatible computers. The BIOS ROM stores the system parameters, such as amount of memory, type of disk drives and video displays, etc. BIOS ROM requires very little power. When the computer is turned off, a back-up battery provides power to the BIOS ROM, enabling it to retain the system parameters. Each time the computer is powered-on, the computer is then configured with the values stored in the BIOS ROM by the system BIOS, which gains control when the computer is powered on.

How To Change the Configuration Data

The configuration data that determines the system parameters may be changed by entering the BIOS Setup utility. This Setup utility can be accessed by pressing <Del> at the appropriate time during system boot.

Starting the Setup Utility

Normally, the only visible POST (Power On Self Test) routine is the memory test. As the memory is being tested, press the <Delete> key to enter the main menu of the BIOS Setup utility. From the main menu, you can access the other setup screens, such as the Chipset and Power menus. Section 4-3 gives detailed descriptions of each parameter setting in the Setup utility.

An AMIBIOS identification string is displayed at the left bottom corner of the screen, below the copyright message.

4-2 BIOS Features

- Supports Plug and Play V1.0A and DMI 2.3
- Supports Intel PCI (Peripheral Component Interconnect) (PME) local bus specification 2.2
- Supports Advanced Power Management (APM) specification v 1.1
- Supports ACPI
- Supports Flash ROM

AMIBIOS supports the LS120 drive made by Matsushita-Kotobuki Electronics Industries Ltd. The LS120:

- Can be used as a boot device
- Is accessible as the next available floppy drive

AMIBIOS supports PC Health Monitoring chips. When a failure occurs in a monitored activity, AMIBIOS can sound an alarm and display a message. The PC Health Monitoring chips monitor:

- CPU temperature
- Chassis intrusion detector
- Five positive voltage inputs
- Four fan speed monitor inputs

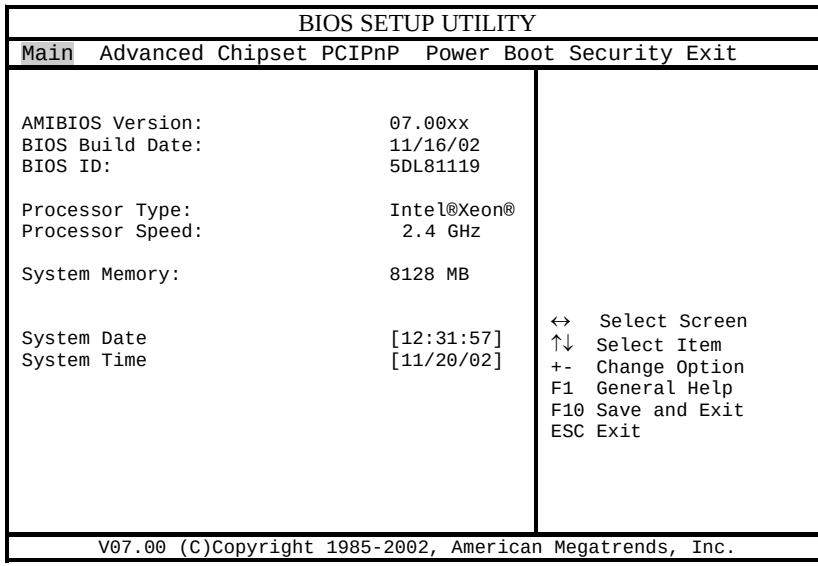
4-3 Running Setup

**Optimal default settings are in bold text unless otherwise noted.*

The BIOS setup options described in this section are selected by choosing the appropriate text from the Standard Setup screen. All displayed text is described in this section, although the screen display is often all you need to understand how to set the options (see on next page).

The Main BIOS Setup Menu

Press the <Delete> key during the POST (Power On Self Test) to enter the Main Menu of the BIOS Setup Utility. All Main Setup options are described in this section. The Main BIOS Setup screeen is displayed below.



Use the Up/Down arrow keys or the <Tab> key to move between the different settings in the above menu.

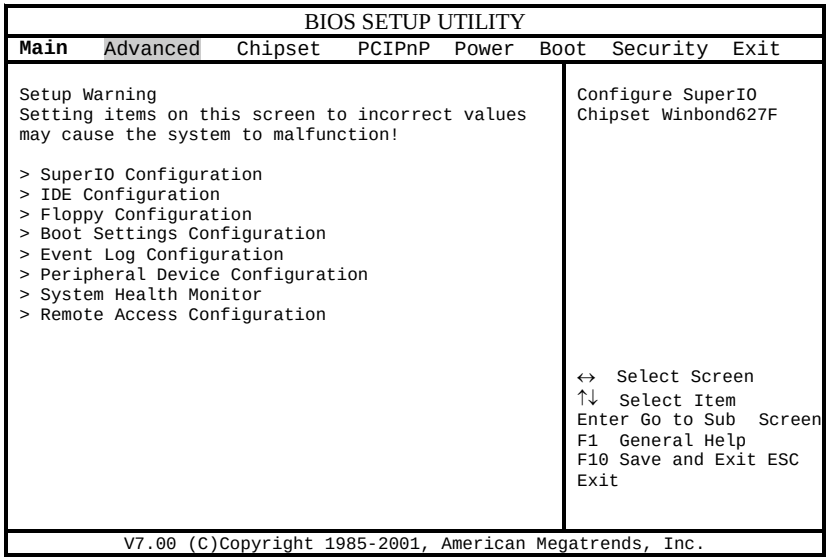
When the items "System Time", and "System Date" are highlighted, type in the correct time/date in the time field, and then press "Enter". The date must be entered in MM/DD/YY format. The time is entered in HH:MM:SS format. The time is in also 24-hour format. For example, 5:30 a.m. appears as 05:30:00 and 5:30 p.m. as 17:30:00.

Press the <ESC> key to exit the Main Menu and use the Left/Right arrow keys to enter the the other categories of BIOS settings. The next section is described in detail to illustrate how to navigate through the menus.

Note: Items displayed in gray are preset and cannot be selected. Items with a blue arrow are commands, not options (i.e. Discard Changes).

4-4 Advanced BIOS Setup

Choose Advanced BIOS Setup from the AMIBIOS Setup Utility main menu with the Left/Right arrow keys. You should see the following display. Select one of the items in the left frame of the screen, such as SuperIO Configuration, to go to the sub screen for that item. Advanced BIOS Setup options are displayed by highlighting the option using the arrow keys. All Advanced BIOS Setup options are described in this section.

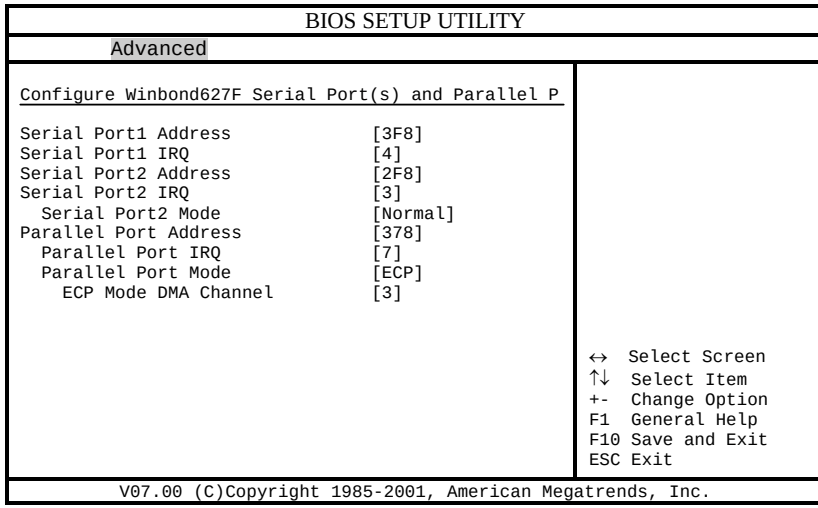


Use the Up/Down arrow keys to select the "Super I/O Configuration line.

When the "Super IO Configuration" line is highlighted, hit "ENTER" to display its menu.

The following Super IO Configuration screen will appear. Here you can select your options for the your computer's I/O (Input/Output) devices.

Super IO Configuration



The Super IO Configuration includes the following items:

Serial Port 1 Address

This option specifies the base I/O port address of serial port 1. The settings for this item include Disabled, **3F8** and 3E8 and 2E8. Select the desired setting and then press "Enter".

Serial Port 1 IRQ

This option specifies the Interrupt Request address of serial port 1. The settings for this item include Disabled, **4** and 3.

Serial Port 2 Address

This option specifies the base I/O port address of serial port 2. The settings for this item include Disabled, **2F8**, 3E8 and 2E8.

Serial Port 2 IRQ

This option specifies the Interrupt Request address of serial port 2. The settings for this item include Disabled, 4 and **3**.

Serial Port 2 Mode

Use this option to choose the Serial Port 2 Mode. The settings are **Normal**, Sharp-IR, SIR and consumer.

Parallel Port Address

This option specifies the I/O address used by the parallel port. The settings for this item include Disabled, **378**, 278 and 3BC. Select your setting and then press "Enter".

Parallel Port IRQ

This option allows the user to set the Parallel Port IRQ. The settings for this item include 5 and **7**.

Parallel Port Mode

This option specifies the parallel port mode. The settings for this item include Normal, Bi-directional, EPP and **ECP**.

ECP Mode DMA Channel

This option allows the user to set the setting for the ECP Mode of the DMA Channel. The settings for this item include **0**, 1 and 3.

IDE Configuration

Onboard PCI IDE Controller

This option allows the user to enable or disable the integrated IDE Controller. The settings include Disabled, Primary, Second and **Both**. Select "Disabled" to disable the Integrated IDE Controller. Select "Primary" to enable the Primary IDE ontroller only. Select "Secondary" to enable the Secondary IDE Controller only. Select "Both" to enable both Primary and Secondary IDE Controllers.

Primary IDE Master

When entering "Setup", BIOS automatically detects the presence of IDE devices. This displays the auto detection status of the IDE devices. You can also manually configure the IDE drives by providing the following information:

This option allows the user to configure the IDE devices. When the desired item is highlighted (selected), press "Enter" and the following screen will be displayed:

Type

This option sets the type of device that the AMIBIOS attempts to boot from after AMIBIOS POST is completed. The settings include Not installed, **Auto**, CDROM and ARMD. The "Auto" setting allows BIOS to automatically detect the presence of the IDE controller.

LBA/Large Mode

LBA (Logical Block Addressing) is a method of addressing data on a disk drive. In LBA mode, the maximum drive capacity is 137 GB. The settings are Disabled and **Auto**. Select "Disabled" to disable LBA mode. Select "Auto" to enable LBA mode if your device supports it and is not already formatted with the LBA mode.

Block (Multi-Sector Transfer) Mode

This option sets the block mode multi sector transfers option The settings include Disabled and **Auto**. Disabled: This option prevents the BIOS from using Multi-Sector Transfer on the specified channel. The data to and from the device will occur one sector at a time. Auto: This option allows the BIOS to auto detect device support for Multi-Sector Transfers on the specified channel. If supported, this option allows the BIOS to auto detect the number of sectors per block for transfer from the hard disk drive to memory. The data transfer to and from the device will occur multiple sectors at a time (if the device supports it).

PIO Mode

IDE PIO (Programmable I/O) mode programs timing cycles between the IDE drive and the programmable IDE controller. As the PIO mode increases, the cycle time decreases. The settings are: **Auto**, 0, 1, 2, 3 and 4.

DMA Mode

This item allows the users to select the DMA mode. The settings are: **Auto**, SWDMA0, SWDMA1, SWDMA2, MWDMA0, MWDMA1, MWDM2, UWDMA0, UWDMA1, UWDMA2, UWDMA3 and UWDMA4. Select Auto to auto detect the DMA Mode. Select SWDMA0 through SWDMA2 to set single word DMA0 through DMA2. Select MWDMA0 through MWDMA2 to set Multi-word DMA0 through DMA2. Select UDMA0 trhough UDMA4 to set Ultra DMA0 through Ultra DMA4.

S.M.A.R.T.

S.M.A.R.T stands for Self-Monitoring Analysis and Reporting Technology, a feature that can help predict impending drive failures. The settings are **Auto**, Disabled and Enabled. Select "Enabled" or "Disabled" to enable or disable the S.M.A.R.T. Select "Auto" to auto detect S.M.A.R.T.

32Bit Data Transfer

The settings are Auto, Disabled and **Enabled**. Select "Enabled" or "Disabled" to enable or disable the 32-bit Data Transfer function. Select "Auto" to auto detect the 32-bit Data Transfer function.

ARMD Emulation Type

This option is used to select the ARMD emulation type used when configuring an LS120, MO (Magneto-Optical), or Iomega Zip drive. The settings are **Auto**, Floppy and HardDisk. (ARMD stands for ATA(PI) Removable Media Disk).

Primary IDE Slave

When the system enters "Setup", BIOS automatically detects the presence of IDE devices. This option displays the auto detection status of IDE devices. The settings for "Primary IDE Slave" are the same as those for the "Primary IDE Master".

Secondary IDE Master

This displays the status of auto detection of IDE devices. The settings for "Secondary IDE Master" are the same as those for the "Primary IDE Master".

Secondary IDE Slave

This displays the status of auto detection of IDE devices. The settings for "Secondary IDE Slave" are the same as those for the "Primary IDE Master".

Hard Disk Write Protect

This item allows the user to prevent the hard disk from being overwritten. The options are Enabled or **Disabled**. Enabled allows the drive to be used normally; read, write and erase functions can all be performed. Disabled prevents the hard disk from being erased. This function is effective only when the device is accessed through BIOS.

ATA(PI) Detect Timeout (Seconds)

Set this option to stop the system search for ATAPI devices within the specified number of seconds. The options are 0, 5, 10, 15, 20, 25, 30 and **35** (seconds). Most ATA disk drives can be detected within 5 seconds.

ATA(PI) 80pin Cable Detection

This option allows you to select the mechanism used to detect the 80-pin ATA(PI) cable. The settings are Host, Device and **Host & Device**.

Floppy Configuration

Floppy A

Use this option to specify which of floppy drive you have installed in the A drive. The settings are Disabled, 360 KB 5 1/4", 1.2 MB 5 1/4", 720 KB 3 1/2", **1.44 MB 3 1/2"** and 2.88 MB 3 1/2".

Floppy B

Use this option to specify which of floppy drive you have installed in the B drive. The settings are Disabled, 360 KB 5 1/4", 1.2 MB 5 1/4", 720 KB 3 1/2", **1.44 MB 3 1/2"** and 2.88 MB 3 1/2".

Diskette Write Protect

This option allows you to prevent any writing to your floppy diskette. The settings are **Disabled,** 360 KB 5 1/4", 1.2 MB 5 1/4", 720 KB 3 1/2", **1.44 MB 3 1/2"** and 2.88 MB 3 1/2". The Enabled setting is effective only if the device is accessed through BIOS.

Floppy Drive Seek

Use this option to Enable or **Disable** the floppy seek routine on bootup.

Boot Settings Configuration

Quick Boot

This option allows the BIOS to skip certain tests that are normally perfomred on boot up. You can disable the option to speed up boot time. The settings are Disabled and **Enabled**.

Quiet Boot

If Disabled, this option will cause the normal POST messages to be displayed upon setup. When Enabled, the OEM logo is displayed instead of the POST messages. The settings are **Enabled** and Disabled.

Add-On ROM Display Mode

Set this option to display add-on ROM (read-only memory) messages. The settings for this option are **Force BIOS** and Keep Current. Force BIOS

allows the computer to force a third party BIOS to display during system boot. Keep Current has the system display AMIBIOS information on bootup.

BootUp Num Lock

This option is used to select the status of the Number Lock function on your keyboard on bootup. The settings are **On** and Off.

BootUp CPU Speed

This option is used set the CPU speed to either **High** or Low.

PS/2 Mouse Support

This option specifies whether a PS/2 Mouse will be supported. Settings are **Enabled** and Disabled.

Typematic Rate

Set this option to select the rate at which the computer repeats a key that is held down. Settings are **Fast** and Slow. Fast: This sets the rate the computer repeats a key to over 20 times per second. Under normal operations, this setting should not be changed. Slow: This sets the rate the computer repeats a key to under 8 times per second.

Primary Display

This option specifies the type of monitor display you have installed on the system. The settings are Absent, **VGA/EGA**, Color 40 x 25, Color 80 x 25 and monochrome.

Parity Check

Use this option to either Enable or **Disable** the use of memory parity checking.

Boot to OS/2

This option can be used to boot the system to an OS/2 operating system. The settings are **No** and Yes.

Wait for F1 if Error

This settings for this option are **Enabled** and Disabled. Disabled: This prevents the AMIBIOS to wait on an error for user intervention. This setting should be used if there is a known reason for a BIOS error to appear. An example would be a system administrator must remote boot the system. The computer system does not have a keyboard currently attached. If this setting is set, the system will continue to bootup in to the operating system. If 'F1' is enabled, the system will wait until the BIOS setup is entered. Enabled: This option allows the system BIOS to wait for any error. If an error is detected, pressing <F1> will enter Setup and the BIOS setting can be adjusted to fix the problem. This normally happens when upgrading the hardware and not setting the BIOS to recognize it.

Hit "Delete" Message Display

This option tells the system to display or not display the "Hit Delete to Enter Setup" message. The settings are **Enabled** and Disabled.

Cache

This option is for enabling or disabling the internal CPU L1 cache. Settings include Disabled, Write-Thru, **Write-Back** and Reserved. Disabled: This option prevents the system from using the internal CPU L1 cache. This setting should be used to slow the computer system down or to trouble-shoot error messages. Write-Thru: This option allows the computer system to use the internal CPU L1 cache as Write-Though cache. Write-Through cache is slower than Write-Back cache. It performs write operations to the internal L1 CPU cache and system memory simultaneously. Write-Back:
This option allows the computer system to use the internal CPU L1 cache as Write-Back cache. Write-Back cache is faster than Write-Through cache. Write-Back cache is a caching method in which modifications to data in the cache aren't copied to the cache source until absolutely necessary. Write-back caching is available on all CPUs supported by this BIOS. With these CPUs, write operations stored in the L1 cache aren't copied to main memory until absolutely necessary. This is the default setting.

System BIOS Cacheable

This option enables you to move the system BIOS to the memory cache to improve performance. Settings are **Enabled** and Disabled.

Event Log Configuration

Event Logging

This option **Enables** or Disables the logging of events. You can use this screen to select options for the Event Log Configuration Settings. You can access sub screens to view the event log and mark all events as read. Use the up and down arrow keys to select an item, and the plus (+) and minus (-) keys to change the option setting. The settings are described on the following pages. The screen is shown below.

ECC Event Logging

This option Enables or **Disables** the logging of ECC events. The events logged by AMIBIOS are post errors such as a bad BIOS, floppy errors, or hard drive errors.

Clear All Event Logs

This option can be used to tell the system to clear the event log on the next boot up. The settings are **No** and Yes.

View Event Log

Highlighting this and pressing <Enter> will allow you to view the unread events from the event log area.

Mark All Events As Read

Highlighting [OK] and pressing <Enter> will mark all events in the log area as having been read. The settings are OK and **Cancel**.

Peripheral Device Configuration

Power Lost Control

This option determines how the system will respond when power is reapplied after a power loss condition. Choose **Always On** to automatically start up the system when power is reapplied. Always Off means you must push the main power button to restart the system after power is restored.

System Health Monitor

The BIOS continuously monitors the health of your system by measuring certain voltage levels and temperatures.

CPU1 Current Temperature/CPU2 Current Temperature

This reading displays the real-time temperatures of CPU1 and CPU2.

System Current Temperature1/System Current Temperature2

This reading displays two real-time temperatures of the system.

Remote Access Configuration

This option allows the user to redirect the console (display) through the COM port when enabled. This is useful when two computers are hooked up to a single monitor. When enabled, the user can toggle the display from one system to the other using the <Tab> key. The function keys are disabled when this setting is enabled. The settings are "Serial ANSI" and "**Disabled**."

4-5 Chipset Setup

Choose Chipset Setup from the AMIBIOS Setup Utility main menu. The screen is shown below. All Chipset Setup options are described following the screen.

```
                        BIOS SETUP UTILITY
Main   Advanced   Chipset   PCIPnP   Power   Boot   Security   Exit

Memory Timing Control          [Auto]              Options for MCH
SDRAM CAS Latency              [CAS Latency 2.5]
MPS 1.4 Support                [Enabled]
Hyper-threading                [Enabled]
Auto DQS Setting Support       [Disabled]
DQS Selection                  [36]
Watch Dog Timer                [Disabled]

                                                   ↔  Select Screen
                                                   ↑↓  Select Item
                                                   Enter Go to Sub  Screen
                                                   F1  General Help
                                                   F10 Save and Exit ESC
                                                   Exit

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```

Memory Timing Control

Determines how the memory timing is controlled. **Auto** lets BIOS program the memory timing from SPD data. Manual allows the user to select the appropriate memory timing.

SDRAM CAS Latency

This sets the CAS latency for system memory. The default setting is **CAS Latency 2.5**.

MPS 1.4 Support

The settings for this option are **Enabled** and Disabled.

Hyper-threading

Enables hyper-threading if supported by the operating system. Hyper-threading is a method of creating an additional "virtual" processor by using parallelism to process mulitple instructions simultaneously. The settings for this option are **Enabled** and Disabled.

Auto DQS Setting Support

The settings for this option are **Disabled** and Enabled.

DQS Selection

This setting is preset.

Watchdog Timer

This option is used to configure the Watchdog timer. Settings are **Disabled**, 2 minutes, 5 minutes, 10 minutes and 15 minutes.

4-6 PCI PnP Setup

Choose PCI/PnP Setup from the AMIBIOS Setup main menu. All PCI/PnP options are described in this section. The PCI/PnP Setup screen is shown below.

```
                        BIOS SETUP UTILITY
Main  Advanced Chipset PCIPnP  Power Boot Security Exit

Plug & Play O/S                 [No]
Reset Config Data               [No]
Allocate IRQ to VGA             [Yes]
PCI IDE BusMaster               [Disabled]

USB Function                    [Enabled]
Legacy USB Support              [Auto]
ARMD Emulation Type             [Hard Disk]

                                ↔   Select Screen
                                ↑↓  Select Item
                                +-  Change Option
                                F1  General Help
                                F10 Save and Exit
                                ESC Exit

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```

Plug & Play OS

This option specifies how Plug and Play devices will be configured. The settins are Yes and **No**. No lets BIOS configure all devices in the system. Yes lets the operating system (if supported) configure PnP devices not required for bootup.

Reset Configuration Data

Choosing the Yes setting will cause the PnP configuration data in the BIOS to be cleared on the next boot up. Choosing the **No** setting does not force PnP data to be cleared on the next boot.

Allocate IRQ to VGA

This option lets you allocate an interrupt request (IRQ) to the PCI VGA adapter card (if used). The settings are **Yes** and No.

PCI IDE BusMaster

The settings for this option are **Disabled** and Enabled. Enable to specify that the IDE controller on the PCI bus has bus mastering capabilities.

USB Function

The settings for this option are Disabled and **Enabled**. Disabled prevents the use of the USB ports and Enabled allows the use of the USB ports.

Legacy USB Support

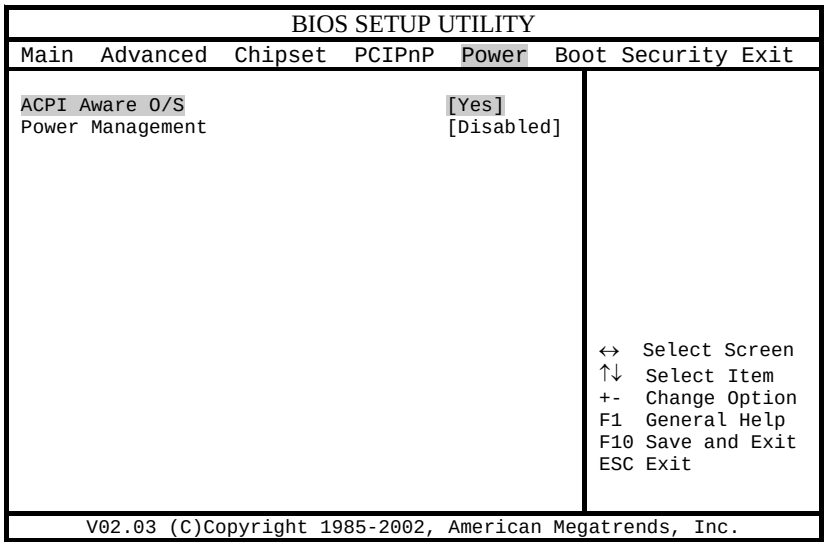
This option allows you to enable support for Legacy USB. The settings are **Auto**, Enabled and Disabled.

ARMD Emulation Type

This settings for this option are **Hard Disk**, Auto and Floppy.

4-7 Power Setup

Choose Power Setup from the AMIBIOS Setup main menu. All Power Setup options are described in this section. The Power Setup screen is shown below.



ACPI Aware O/S

This option allows the system to utilize Intel's ACPI (Advanced Configuration and Power Interface) specification. Settings are No and **Yes**. DOS®, Windows 3.x®, and Windows NT® are examples of non-ACPI aware operating systems. Windows 95®, Windows 98®, Windows ME® and Windows 2000® are examples of ACPI aware operating systems.

Power Management

When enabled, this option displays the following four options relating to power management. The settings are **Disabled** and Enabled.

Power Button Mode

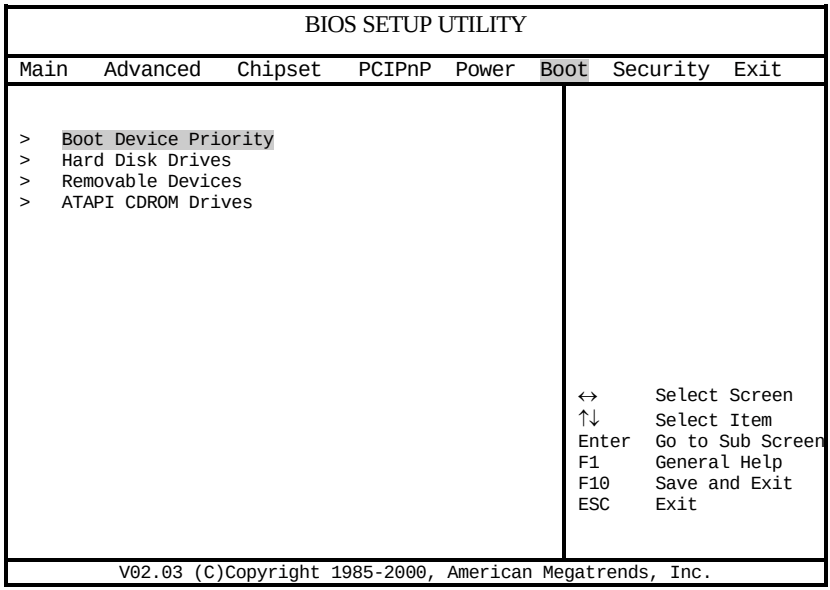
This option allows you to change the function of the chassis power button. The settings are **On/Off** and Suspend. When set to Suspend, depressing the power button when the system is up will cause it to enter a suspend state.

Suspend Timeout

This option specifies the length of hard disk inactivity time that should expire before entering the power conserving state. The settings are **Off**, 1, 2, 3, 4, 5, 6, 7, 8, 9 and 10 (minutes).

4-8 Boot Setup

Choose Boot Setup from the AMIBIOS Setup main menu. All Boot Setup options are described in this section. The Boot Setup screen is shown below.



Boot Device Priority

1st Boot Device

This option is used to specify the order of the boot sequence that will be followed from the available system devices. The settings for the 1st Boot Device are **Removable Device**, ATAPI CDROM, Hard Drive, Onboard LAN2 Option-ROM and IBA 4.0.1.9 Slot 0102.

2nd Boot Device

The settings for the 2nd Boot Device are Removable Device, **ATAPI CDROM**, Hard Drive, Onboard LAN2 Option-ROM and IBA 4.0.1.9 Slot 0102.

3rd Boot Device

The settings for the 3rd Boot Device are Removable Device, ATAPI CDROM, **Hard Drive**, Onboard LAN2 Option-ROM and IBA 4.0.1.9 Slot 0102.

4th Boot Device

The settings for the 4th Boot Device are Removable Device, ATAPI CDROM, Hard Drive, **Onboard LAN2 Option-ROM** and IBA 4.0.1.9 Slot 0102.

5th Boot Device

The settings for the 5th Boot Device are Removable Device, ATAPI CDROM, Hard Drive, Onboard LAN2 Option-ROM and **IBA 4.0.1.9 Slot 0102**.

Hard Disk Drives

Use this screen to view the boot sequency of hard drives that have been auto-detected or entered manually on your system.

Removable Devices

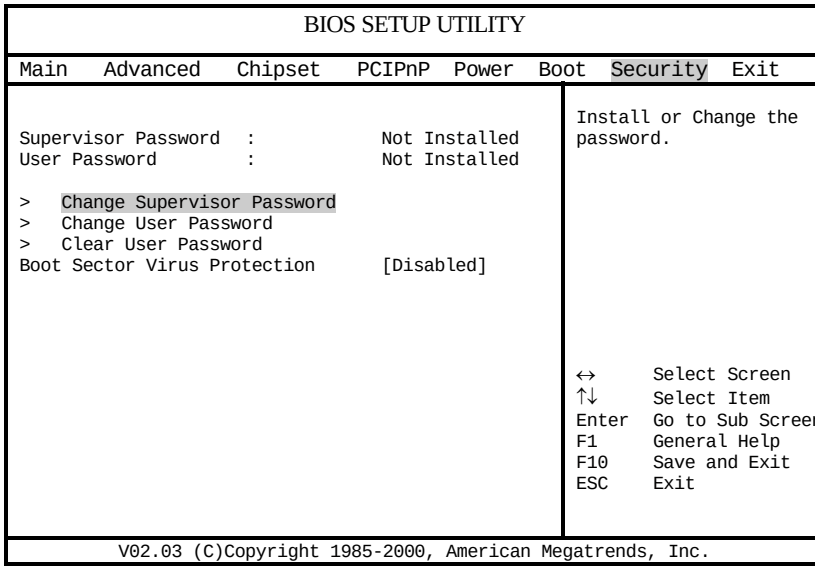
Use this screen to view the boot sequency of the removeable devices that have been auto-detected or entered manually on your system.

ATAPI CDROM Drives

Use this screen to view the boot sequency ofthe ATAPI CDROM drives that have been auto-detected or entered manually on your system.

4-9 Security Setup

Choose Security Setup from the AMIBIOS Setup main menu. All Security Setup options are described in this section. The Security Setup screen is shown below.



Supervisor Password

User Password

AMIBIOS provides both Supervisor and User password functions. If you use both passwords, the Supervisor password must be set first. The system can be configured so that all users must enter a password every time the system boots or when AMIBIOS Setup is executed, using either or both the Supervisor password or User password. The Supervisor and User passwords activate two different levels of password security. If you select password support, you are prompted for a 1 – 6 character password. Type the password on the keyboard. The password does not appear on the screen when typed. Make sure you write it down. If you forget it, you must clear CMOS and reconfigure. **Remember your Password!** Keep a record of the new password when the password is changed. If you forget the password, you must erase the system configuration information in CMOS.

Change Supervisor Password

This option allows you to change a supervisor password that was entered previously.

Change User Password

This option allows you to change a user password that was entered previously.

Clear User Password

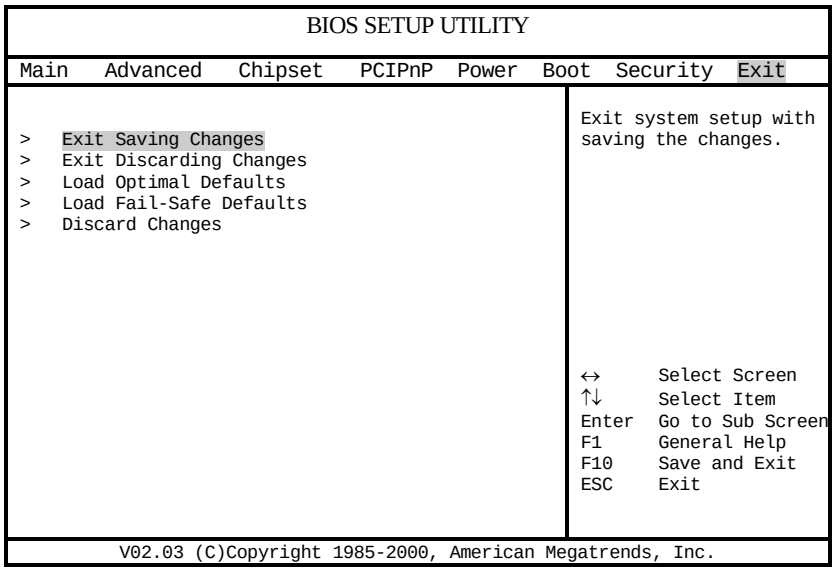
Use this option to clear the user password so that it is not required to be entered when the system boots up.

Boot Sector Virus Protection

This option allows you to enable or disable a virus detection program to protect the boot sector of your hard disk drive. The settings for this option **Disabled** and Enabled. If Enabled, AMIBIOS will display a warning when any program (or virus) issues a Disk Format command or attempts to write to the boot sector of the hard disk drive.

4-10 Exit Setup

Choose Exit Setup from the AMIBIOS Setup main menu. All Exit Setup options are described in this section. The Exit Setup screen is shown below.



Exit Saving Changes

Highlighting this setting and then pressing <Enter> will save any changes you made in the BIOS Setup program and then exit. Your system should then continue with the boot up procedure.

Exit Discarding Changes

Highlighting this setting and then pressing <Enter> will ignore any changes you made in the BIOS Setup program and then exit. Your system should then continue with the boot up procedure.

Load Optimal Defaults

Highlighting this setting and then pressing <Enter> provides the optimum performance settings for all devices and system features.

Load Failsafe Defaults

Highlighting this setting and then pressing <Enter> provides the safest set of parameters for the system. Use them if the system is behaving erratically.

Discard Changes

Highlighting this setting and then pressing <Enter> will ignore any changes you made in the BIOS Setup program but will not exit the BIOS Setup program.

Notes

Appendix A
BIOS Error Beep Codes

During the POST (Power-On Self-Test) routines, which are performed each time the system is powered on, errors may occur.

Non-fatal errors are those which, in most cases, allow the system to continue the boot-up process. The error messages normally appear on the screen.

Fatal errors are those which will not allow the system to continue the boot-up procedure. If a fatal error occurs, you should consult with your system manufacturer for possible repairs.

These fatal errors are usually communicated through a series of audible beeps. The numbers on the fatal error list, on the following page, correspond to the number of beeps for the corresponding error. All errors listed, with the exception of Beep Code 8, are fatal errors.

POST codes may be read on the debug LEDs located beside the LAN port on the motherboard backplane. See the description of the Debug LEDs (LED1 and LED2) in Section 2-6.

A-1 AMIBIOS Error Beep Codes

Beep Code	Error Message	Description
1 beep	Refresh	Circuits have been reset. (Ready to power up.)
5 short, 1 long	Memory error	No memory detected in system
8 beeps	Display memory read/write error	Video adapter missing or with faulty memory

Notes

Appendix B
BIOS POST Checkpoint Codes

When AMIBIOS performs the Power On Self Test, it writes checkpoint codes to I/O port 0080h. If the computer cannot complete the boot process, diagnostic equipment can be attached to the computer to read I/O port 0080h.

B-1 Uncompressed Initialization Codes

The uncompressed initialization checkpoint codes are listed in order of execution:

Checkpoint	Code Description
D0h	The NMI is disabled. Power on delay is starting. Next, the initialization code checksum will be verified.
D1h	Initializing the DMA controller, performing the keyboard controller BAT test, starting memory refresh, and entering 4 GB flat mode next.
D3h	Starting memory sizing next.
D4h	Returning to real mode. Executing any OEM patches and setting the Stack next.
D5h	Passing control to the uncompressed code in shadow RAM at E000:0000h. The initialization code is copied to segment 0 and control will be transferred to segment 0.
D6h	Control is in segment 0. Next, checking if <Ctrl> <Home> was pressed and verifying the system BIOS checksum. If either <Ctrl> <Home> was pressed or the system BIOS checksum is bad, next will go to checkpoint code E0h. Otherwise, going to checkpoint code D7h.

B-2 Bootblock Recovery Codes

The bootblock recovery checkpoint codes are listed in order of execution:

Checkpoint	Code Description
E0h	The onboard floppy controller if available is initialized. Next, beginning the base 512 KB memory test.
E1h	Initializing the interrupt vector table next.
E2h	Initializing the DMA and Interrupt controllers next.
E6h	Enabling the floppy drive controller and Timer IRQs. Enabling internal cache memory.
Edh	Initializing the floppy drive.
Eeh	Looking for a floppy diskette in drive A:. Reading the first sector of the diskette.
Efh	A read error occurred while reading the floppy drive in drive A:.
F0h	Next, searching for the AMIBOOT.ROM file in the root directory.
F1h	The AMIBOOT.ROM file is not in the root directory.
F2h	Next, reading and analyzing the floppy diskette FAT to find the clusters occupied by the AMIBOOT.ROM file.
F3h	Next, reading the AMIBOOT.ROM file, cluster by cluster.
F4h	The AMIBOOT.ROM file is not the correct size.
F5h	Next, disabling internal cache memory.
FBh	Next, detecting the type of flash ROM.
FCh	Next, erasing the flash ROM.
FDh	Next, programming the flash ROM.
FFh	Flash ROM programming was successful. Next, restarting the system BIOS.

B-3 Uncompressed Initialization Codes

The following runtime checkpoint codes are listed in order of execution. These codes are uncompressed in F0000h shadow RAM.

Checkpoint	Code Description
03h	The NMI is disabled. Next, checking for a soft reset or a power on condition.
05h	The BIOS stack has been built. Next, disabling cache memory.
06h	Uncompressing the POST code next.
07h	Next, initializing the CPU and the CPU data area.
08h	The CMOS checksum calculation is done next.
0Ah	The CMOS checksum calculation is done. Initializing the CMOS status register for date and time next.
0Bh	The CMOS status register is initialized. Next, performing any required

	initialization before the keyboard BAT command is issued.
0Ch	The keyboard controller input buffer is free. Next, issuing the BAT command to the keyboard controller.
0Eh	The keyboard controller BAT command result has been verified. Next, performing any necessary initialization after the keyboard controller BAT command test.
0Fh	The initialization after the keyboard controller BAT command test is done. The keyboard command byte is written next.
10h	The keyboard controller command byte is written. Next, issuing the Pin 23 and 24 blocking and unblocking command.
11h	Next, checking if <End or <Ins> keys were pressed during power on. Initializing CMOS RAM if the *Initialize CMOS RAM in every boot* AMIBIOS POST option was set in AMIBCP or the <End> key was pressed.
12h	Next, disabling DMA controllers 1 and 2 and interrupt controllers 1 and 2.
13h	The video display has been disabled. Port B has been initialized. Next, initializing the chipset.
14h	The 8254 timer test will begin next.
19h	The 8254 timer test is over. Starting the memory refresh test next.
1Ah	The memory refresh line is toggling. Checking the 15 second on/off time next.
2Bh	Passing control to the video ROM to perform any required configuration before the video ROM test.
2Ch	All necessary processing before passing control to the video ROM is done. Looking for the video ROM next and passing control to it.
2Dh	The video ROM has returned control to BIOS POST. Performing any required processing after the video ROM had control.
23h	Reading the 8042 input port and disabling the MEGAKEY Green PC feature next. Making the BIOS code segment writable and performing any necessary configuration before initializing the interrupt vectors.
24h	The configuration required before interrupt vector initialization has completed. Interrupt vector initialization is about to begin.

Checkpoint Code	Description
25h	Interrupt vector initialization is done. Clearing the password if the POST DIAG switch is on.
27h	Any initialization before setting video mode will be done next.
28h	Initialization before setting the video mode is complete. Configuring the monochrome mode and color mode settings next.
2Ah	Bus initialization system, static, output devices will be done next, if present. See the last page for additional information.
2Eh	Completed post-video ROM test processing. If the EGA/VGA controller is not found, performing the display memory read/write test next.
2Fh	The EGA/VGA controller was not found. The display memory read/write test is about to begin.
30h	The display memory read/write test passed. Look for retrace checking next.
31h	The display memory read/write test or retrace checking failed. Performing the alternate display memory read/write test next.
32h	The alternate display memory read/write test passed. Looking for alternate display retrace checking next.
34h	Video display checking is over. Setting the display mode next.
37h	The display mode is set. Displaying the power on message next.
38h	Initializing the bus input, IPL, general devices next, if present. See the last page of this chapter for additional information.
39h	Displaying bus initialization error messages. See the last page of this chapter for additional information.
3Ah	The new cursor position has been read and saved. Displaying the *Hit <DEL>* message next.
3Bh	The *Hit <DEL>* message is displayed. The protected mode memory test is about to start.
40h	Preparing the descriptor tables next.
42h	The descriptor tables are prepared. Entering protected mode for the memory test next.
43h	Entered protected mode. Enabling interrupts for diagnostics mode next.
44h	Interrupts enabled if the diagnostics switch is on. Initializing data to check memory wraparound at 0:0 next.
45h	Data initialized. Checking for memory wraparound at 0:0 and finding the total system memory size next.
46h	The memory wraparound test is done. Memory size calculation has been done. Writing patterns to test memory next.
47h	The memory pattern has been written to extended memory. Writing patterns to the base 640 KB memory next.

Checkpoint	Code Description
48h	Patterns written in base memory. Determining the amount of memory below 1 MB next.
49h	The amount of memory below 1 MB has been found and verified. Determining the amount of memory above 1 MB memory next.
4Bh	The amount of memory above 1 MB has been found and verified. Checking for a soft reset and clearing the memory below 1 MB for the soft reset next. If this is a power on situation, going to checkpoint 4Eh next.
4Ch	The memory below 1 MB has been cleared via a soft reset. Clearing the memory above 1 MB next.
4Dh	The memory above 1 MB has been cleared via a soft reset. Saving the memory size next. Going to checkpoint 52h next.
4Eh	The memory test started, but not as the result of a soft reset. Displaying the first 64 KB memory size next.
4Fh	The memory size display has started. The display is updated during the memory test. Performing the sequential and random memory test next.
50h	The memory below 1 MB has been tested and initialized. Adjusting the displayed memory size for relocation and shadowing next.
51h	The memory size display was adjusted for relocation and shadowing. Testing the memory above 1 MB next.
52h	The memory above 1 MB has been tested and initialized. Saving the memory size information next.
53h	The memory size information and the CPU registers are saved. Entering real mode next.
54h	Shutdown was successful. The CPU is in real mode. Disabling the Gate A20 line, parity, and the NMI next.
57h	The A20 address line, parity, and the NMI are disabled. Adjusting the memory size depending on relocation and shadowing next.
58h	The memory size was adjusted for relocation and shadowing. Clearing the *Hit <DEL>* message next.
59h	The *Hit <DEL>* message is cleared. The *<WAIT...>* message is displayed. Starting the DMA and interrupt controller test next.

Checkpoint	Code Description
60h	The DMA page register test passed. Performing the DMA Controller 1 base register test next.
62h	The DMA controller 1 base register test passed. Performing the DMA controller 2 base register test next.
65h	The DMA controller 2 base register test passed. Programming DMA controllers 1 and 2 next.
66h	Completed programming DMA controllers 1 and 2. Initializing the 8259 interrupt controller next.
67h	Completed 8259 interrupt controller initialization.
7Fh	Extended NMI source enabling is in progress.
80h	The keyboard test has started. Clearing the output buffer and checking for stuck keys. Issuing the keyboard reset command next.
81h	A keyboard reset error or stuck key was found. Issuing the keyboard controller interface test command next.
82h	The keyboard controller interface test completed. Writing the command byte and initializing the circular buffer next.
83h	The command byte was written and global data initialization has completed. Checking for a locked key next.
84h	Locked key checking is over. Checking for a memory size mismatch with CMOS RAM data next.
85h	The memory size check is done. Displaying a soft error and checking for a password or bypassing WINBIOS Setup next.
86h	The password was checked. Performing any required programming before WINBIOS Setup next.
87h	The programming before WINBIOS Setup has completed. Uncompressing the WINBIOS Setup code and executing the AMIBIOS Setup or WINBIOS Setup utility next.
88h	Returned from WINBIOS Setup and cleared the screen. Performing any necessary programming after WINBIOS Setup next.
89h	The programming after WINBIOS Setup has completed. Displaying the power on screen message next.
8Bh	The first screen message has been displayed. The <*WAIT...*> message is displayed. Performing the PS/2 mouse check and extended BIOS data area allocation check next.
8Ch	Programming the WINBIOS Setup options next.
8Dh	The WINBIOS Setup options are programmed. Resetting the hard disk controller next.
8Fh	The hard disk controller has been reset. Configuring the floppy drive controller next.
91h	The floppy drive controller has been configured. Configuring the hard disk drive controller next.

Checkpoint	Code Description
95h	Initializing the bus option ROMs from C800 next. See the last page of this chapter for additional information.
96h	Initializing before passing control to the adaptor ROM at C800.
97h	Initialization before the C800 adaptor ROM gains control has completed. The adaptor ROM check is next.
98h	The adaptor ROM had control and has now returned control to BIOS POST. Performing any required processing after the option ROM returned control.
99h	Any initialization required after the option ROM test has completed. Configuring the timer data area and printer base address next.
9Ah	Set the timer and printer base addresses. Setting the RS-232 base address next.
9Bh	Returned after setting the RS-232 base address. Performing any required initialization before the Coprocessor test next.
9Ch	Required initialization before the Coprocessor test is over. Initializing the Coprocessor next.
9Dh	Coprocessor initialized. Performing any required initialization after the Coprocessor test next.
9Eh	Initialization after the Coprocessor test is complete. Checking the extended keyboard, keyboard ID, and Num Lock key next. Issuing the keyboard ID command next.
A2h	Displaying any soft errors next.
A3h	The soft error display has completed. Setting the keyboard typematic rate next.
A4h	The keyboard typematic rate is set. Programming the memory wait states next.
A5h	Memory wait state programming is over. Clearing the screen and enabling parity and the NMI next.
A7h	NMI and parity enabled. Performing any initialization required before passing control to the adaptor ROM at E000 next.
A8h	Initialization before passing control to the adaptor ROM at E000h completed. Passing control to the adaptor ROM at E000h next.
A9h	Returned from adaptor ROM at E000h control. Performing any initialization required after the E000 option ROM had control next.
Aah	Initialization after E000 option ROM control has completed. Displaying the system configuration next.
Abh	Uncompressing the DMI data and executing DMI POST initialization next.
B0h	The system configuration is displayed.
B1h	Copying any code to specific areas.
00h	Code copying to specific areas is done. Passing control to INT 19h boot loader next.

Notes